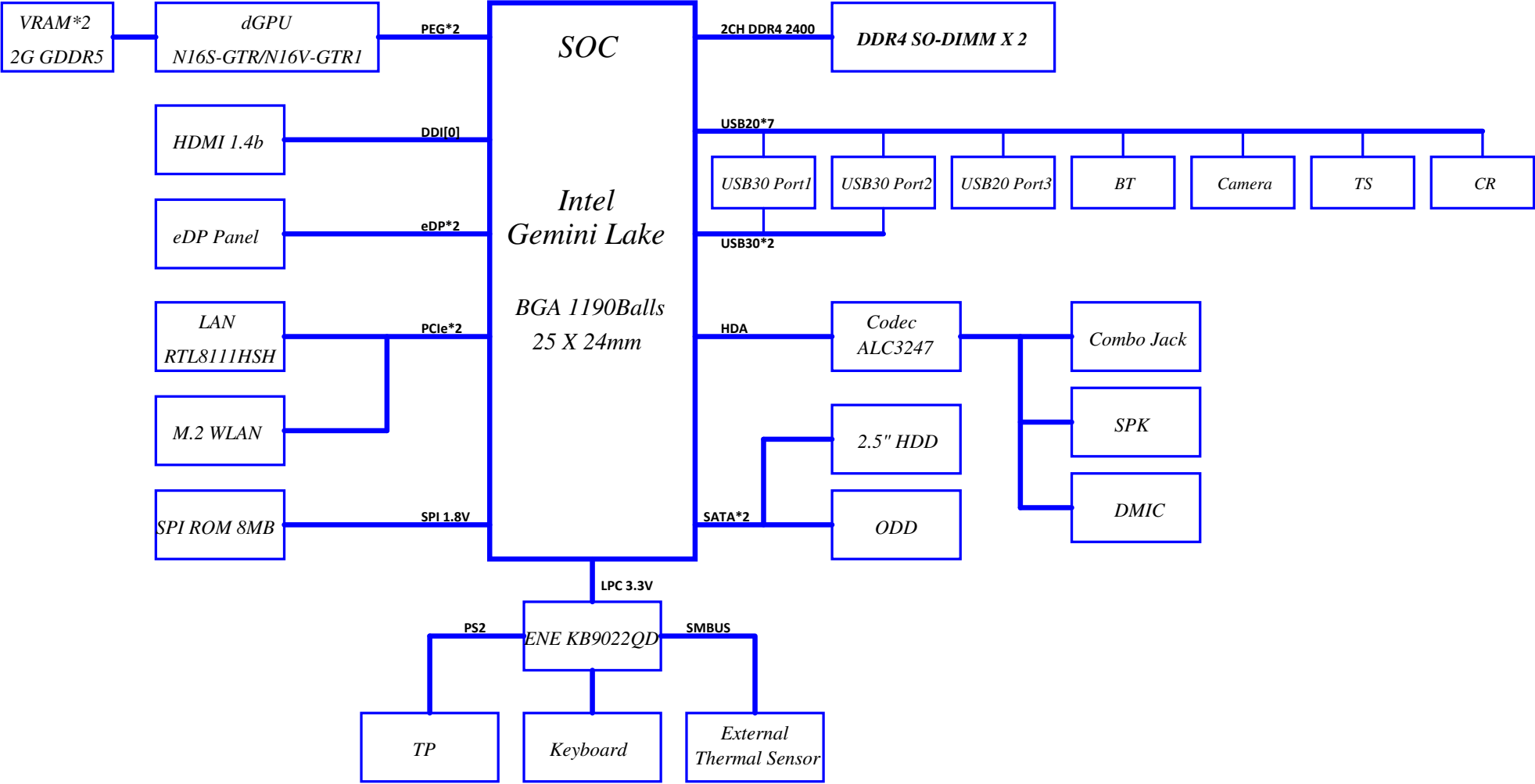


Compal LA-G073P
EPG50
Harry Potter
Intel Gemini Lake + nVidia MX110/130 Schematic
2017-11-05
Rev 0.2

Security Classification		Compal Secret Data		Title	
Issued Date		2015/06/09	Deciphered Date	2016/12/31	2016/12/31
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	
				LA-G073P	
				Date:	Thursday, November 23, 2017
				Sheet	1 of 44
				Rev	0.2



BOM Config

Function	Stuff	Un-Stuff
Keystone SKU	KS@	
Corith SKU	CR@	@CR@
CMC	CMC@	
ME Connector	CONN@	
EMMC	EMMC@	
not CMC	NCMC@	
EMI Components	EMI@	@EMI@
ESD Components	ESD@	@ESD@
RF Components	RF@	@RF@
EC control	EC@	
BIOS control	BIOS@	
NC Components		@

HSIO Port Table

Port	USB3.0	PCIE	SATA	DESTINATION
0	USB3.0-0			USB30 Port1
1	USB3.0-1			USB30 Port2
2				NA
3				NA
4		PCIE-3		WLAN
5		PCIE-2		LAN
6		PCIE-1		dGPU
7		PCIE-0		dGPU
8			SATA-1	ODD
9			SATA-0	2.5" HDD

USB2.0 Port Table

USB2.0 Port	Device
0	USB30 Port1
1	USB30 Port2
2	USB20 Port(S/B)
3	BT
4	Camera
5	TS
6	CR
7	NA

Power State

STATE	SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	+VALW	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)		HIGH	LOW	HIGH	ON	OFF	OFF
S4 (Suspend to Disk)		HIGH	LOW	LOW	ON	OFF	OFF

SOC SMBUS Address Table

SOC_SMBUS Net Name	Power Rail	Device	Address (8 bit)
SOC_SMBCLK SOC_SMBDATA	+3VALW_SOC	DIMM1 DIMM2	0xA0 0xA4
	+3VALW_SOC	Touch Pad	TBC
	+1.8VALW	XDP connector	TBC

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)
SMBUS Port 1	+3VALW_EC	BAT	TBC
		CHGR	TBC
SMBUS Port 2	+3VS	dGPU	TBC
		Thermal Sensor	0x4C

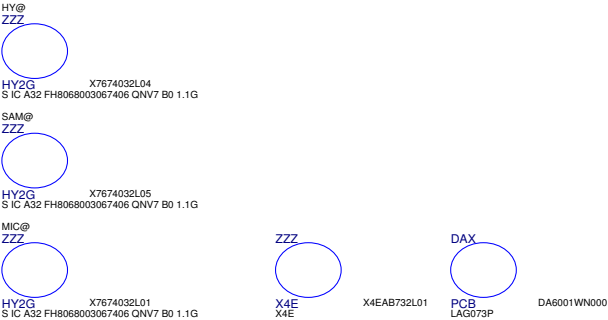
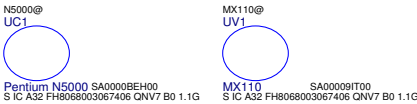


Figure 31-1. High Speed I/O (HSIO) Lane Multiplexing in GLK SoC



Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5
VIN	Adapter power supply	ON	ON	ON	ON
BATT+	Battery power supply	ON	ON	ON	ON
+VBATA	AC or battery power rail for power circuit	ON	ON	ON	ON
+VNN	Core voltage for CPU	ON	OFF	OFF	OFF
+VCCGI	Graphics Core and ISP logic power rail	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	Fixed voltage rail for SRAM and I/O Logic	ON	OFF	OFF	OFF
+1.24V_1.35VALW_SOC	SoC L2, I/O Logic and PLLs	ON	ON	ON	OFF
+1.2V_DDR	DDRIII/L-RS +1.2V power rail	ON	ON	ON	OFF
+2.5V_DDR	DDRIII/L-RS +1.8V power rail	ON	ON	ON	OFF
+1.8VALW	For SoC and System +1.8V power rail	ON	ON	ON	OFF
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON
+3VL	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+3VS	System +3VS power rail	ON	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON
+5VS	System +5VS power rail	ON	ON	OFF	OFF

[Gemini Lake-PowerMap]

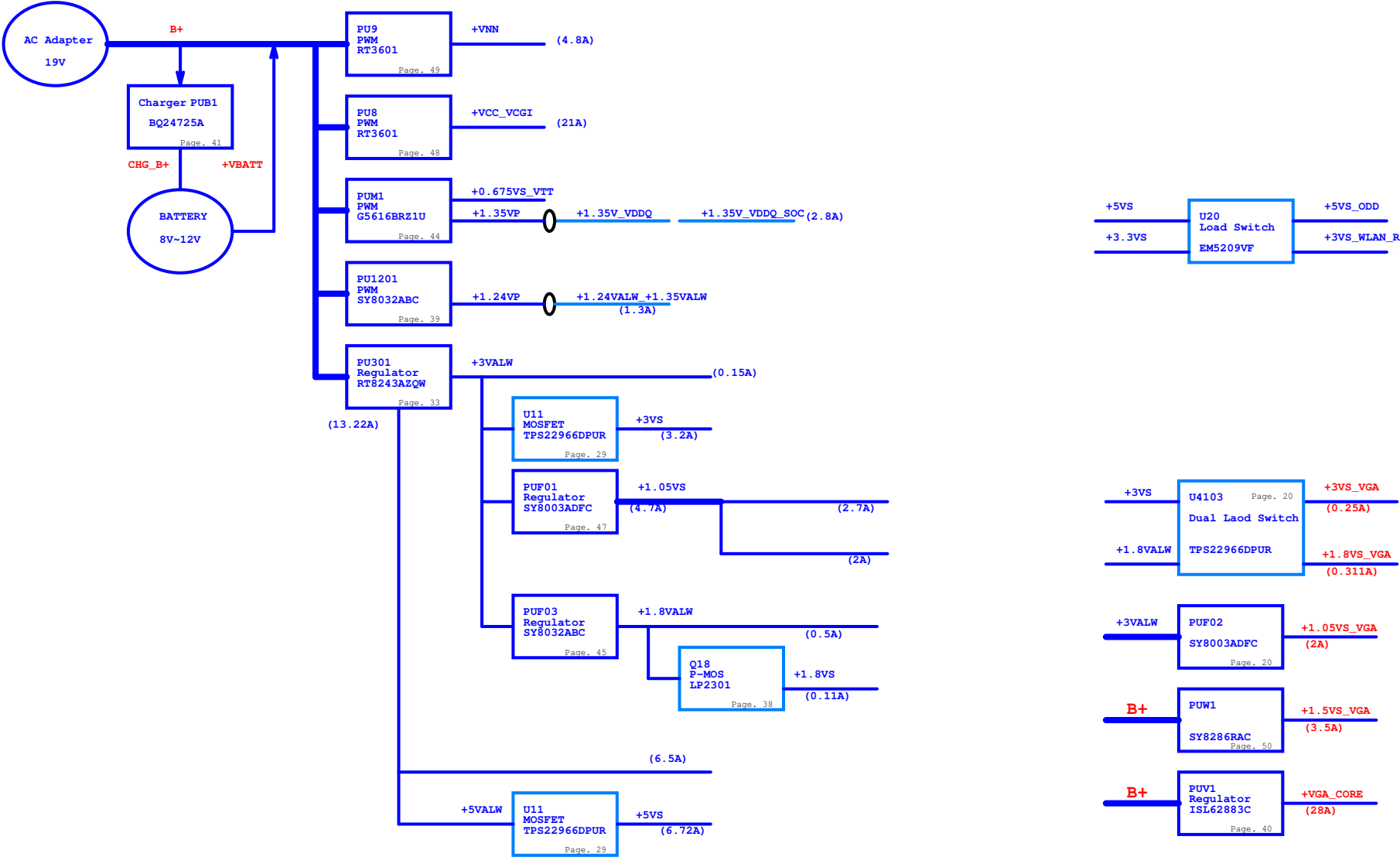
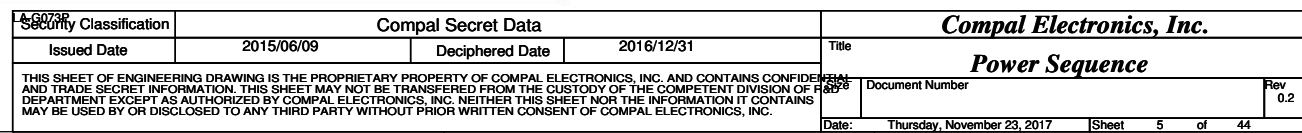
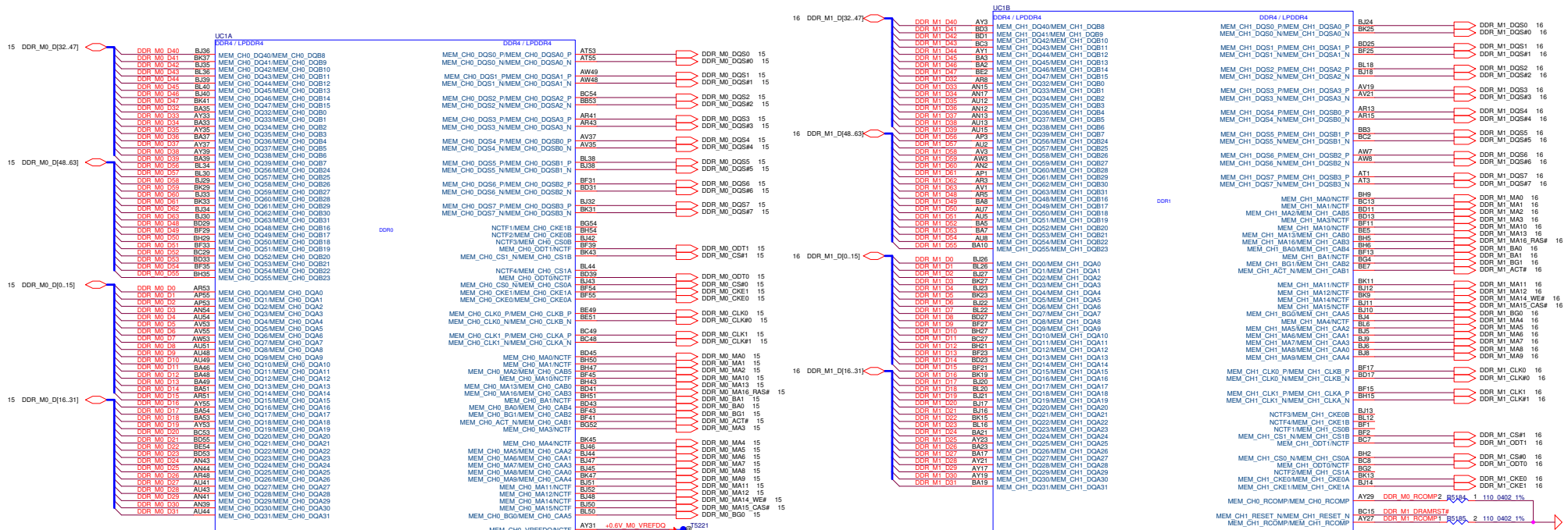
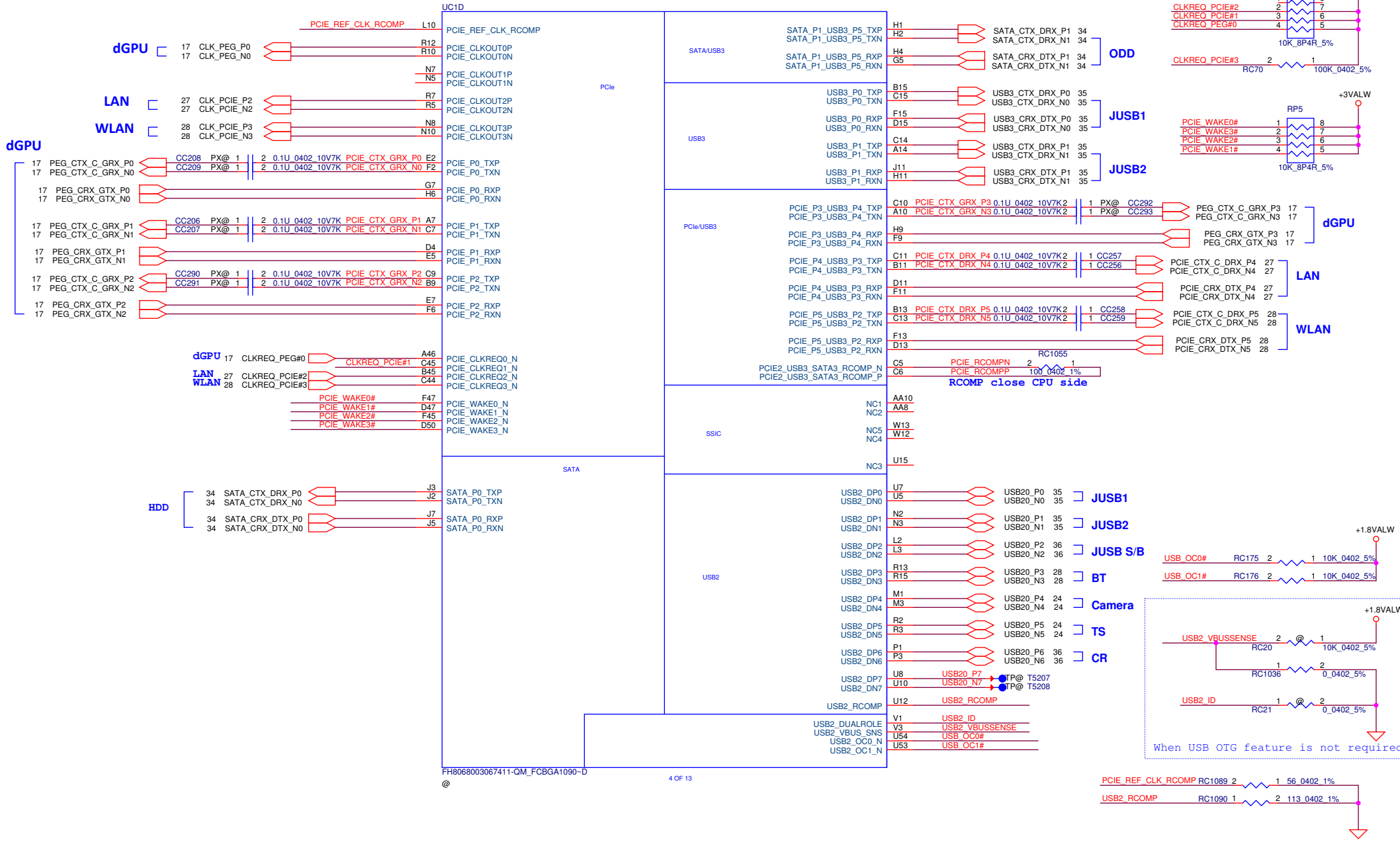


Figure 4-30. G3 -> S0 (Adapter)

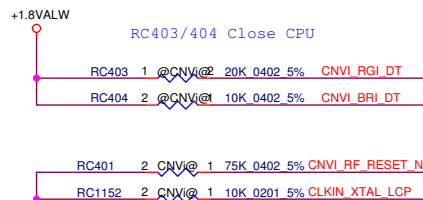
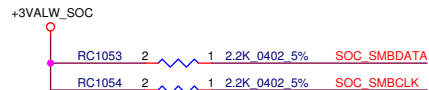




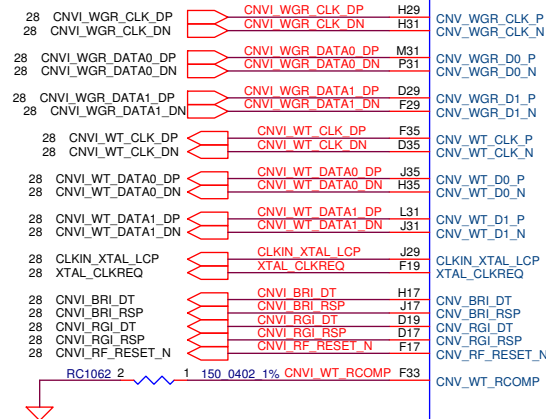
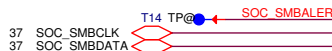
1 OF 13 2 OF 13



Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2015/06/09		Deciphered Date		2016/12/31		Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						GML(4/9)USB2/3,PCIE,SATA					
						Document Number				Rev	
						LA-G073P				0.2	
						Date:		Thursday, November 23, 2017		Sheet 9 of 44	



SMBus 1.8V/3.3V selection is done by hardware strap GPIO_163



UC11

U49
U51 SIO_I2C0_SCL
SIO_I2C0_SDA

U46
U48 SIO_I2C1_SCL
SIO_I2C1_SDA

AA39
AA41 SIO_I2C2_SCL
SIO_I2C2_SDA

R44
R43 SIO_I2C3_SCL
SIO_I2C3_SDA

R49
R51 SIO_I2C4_SCL
SIO_I2C4_SDA

C50
A50 SIO_I2C5_SCL
SIO_I2C5_SDA

C48
C47 SIO_I2C6_SCL
SIO_I2C6_SDA

B47
C46 SIO_I2C7_SCL
SIO_I2C7_SDA

SMB_ALERT_N

SMB_CLK

SMB_DATA

LPSS_I2C

LPSS SMBus

CNVi

FH8068003067411-QM_FCBGA1090-D

6 OF 13

LPSS_SPI

SIO_SPI_0_CLK

SIO_SPI_0_TXD

SIO_SPI_0_RXD

SIO_SPI_0_FS0

SIO_SPI_0_FS1

SIO_SPI_2_CLK

SIO_SPI_2_TXD

SIO_SPI_2_RXD

SIO_SPI_2_FS0

SIO_SPI_2_FS1

SIO_SPI_2_FS2

SIO_UART0_TXD

SIO_UART0_RXD

SIO_UART0_RTS_N

SIO_UART0_CTS_N

SIO_UART2_TXD

SIO_UART2_RXD

SIO_UART2_RTS_N

SIO_UART2_CTS_N

M39

J37

L39

L37

J39

M37

M33

P35

P33

P37

L35

N54

P53

N53

M55

L54

M53

K53

L53

SPI_0_TX_GPIO_83 11

SPI_0_FS0_GPIO_80 11

SPI_0_FS1_GPIO_81 33

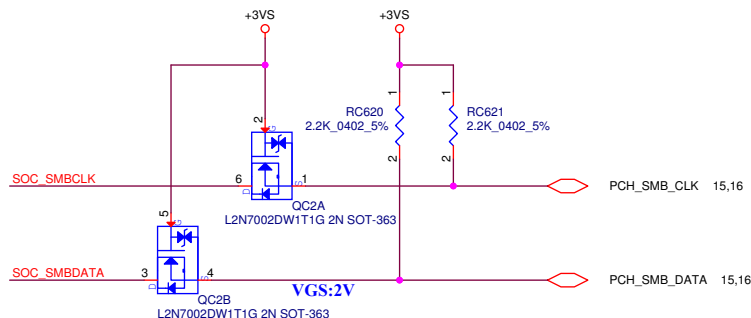
SPI_2_CLK_GPIO_84 11

UART_0_CTXD_GPIO_61 11

UART_2_CTXD_GPIO_65 11,28

UART_2_CRXD_GPIO_64 28

UART_2_CRTS#_GPIO_66 10K 0402 5% 2 1 RC1111



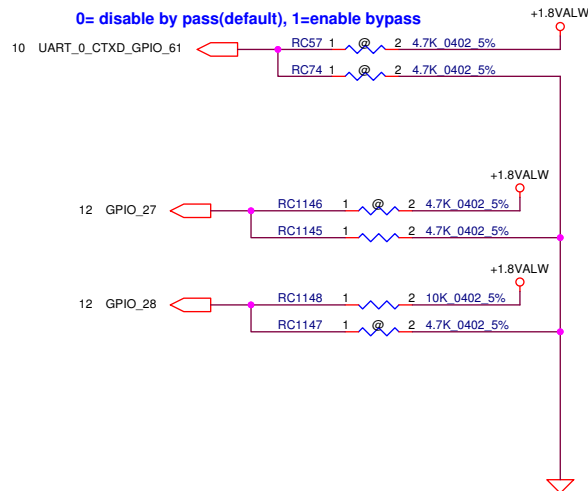
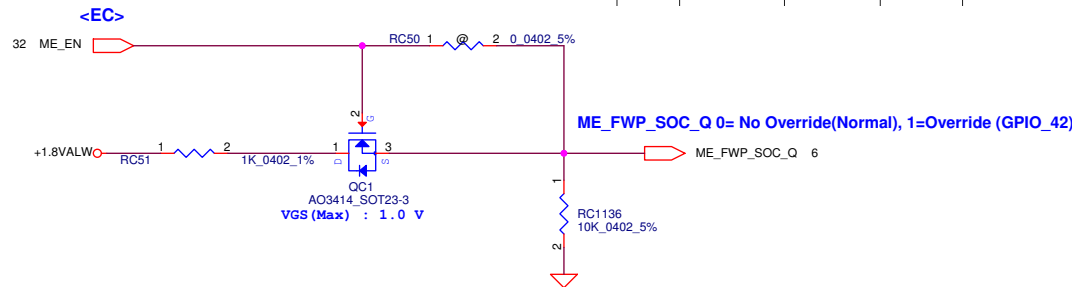
Security Classification	Compal Secret Data			Notice:
Issued Date	2015/06/09	Deciphered Date	2016/12/31	SIO_EXT#1 (2015 PD)
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				STO_EXT#1 WAKE#
				Document Number
				LA-G073P
				Rev 0.2
				Date: Thursday, November 23, 2017
				Sheet 10 of 44

GPIO_86	SIO_SPI_2_FS1	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_87	SIO_SPI_2_FS2	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_89	SIO_SPI_2_TXD	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_159	AVS_I2S0_S0I	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_163	AVS_I2S1_WS_SY NC	SMBus 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_164	AVS_I2S1_S0I	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_168	AVS_HDA_S0I	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_172	AVS_M_CLK_B1	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) Note: Platforms should strap this LOW. Functionality is handled by the PMC.
GPIO_174	AVS_M_CLK_AB2	VDD2 1.24V vs. 1.20V select	20K PD	1=VDD2 is 1.24V; 0=VDD2 is 1.20V (default)

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_27	GPIO_27	Allow eMMC as a boot source	20K PU	1=enable (default); 0=disable; If platform is using SPI as the boot device, then provide a pull-down for this strap to disable eMMC
GPIO_28	GPIO_28	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable Note: If platform is using eMMC as boot device, then provide a pull down for this strap to disable SPI.
GPIO_42	MDS1_A_TE	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override Note: This strap enables the platform to override security features in the SPI.
GPIO_43	MDS1_C_TE	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_44	USB2_OC0_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_45	USB2_OC1_N	Top swap override	20K PD	1 = Enable 0 = Disable (default) Note: Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_61	SIO_UART0_TXD	Enable TXE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) Note: This strap tells TXE 3.0 to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of TXE3.0 before the first patch point this strap enabled the platform tell TXE 3.0 to bypass the ROM causing the issue and go to the patch space instead.
GPIO_62	SIO_UART0_RTS_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

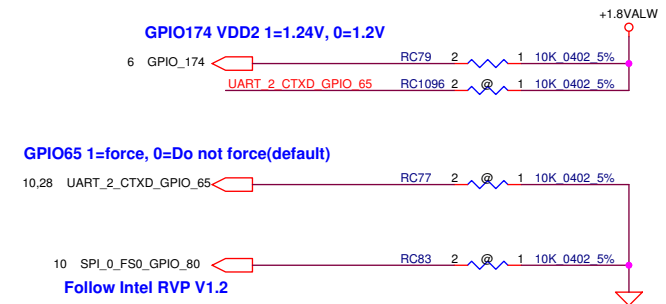
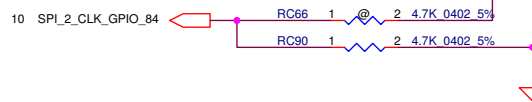
GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_65	SIO_UART2_TXD	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) Notes: 1- DNX: Download and Execute 2- This strap is a recovery strap for corrupted FW image. This strap will force TXE3.0 to execute a "Download and Execute" (DNX) flow, where it would download a new firmware image from a recovery host, over USB, and overwrite the image in the storage media. TXE can do it for BIOS part of FW, but if TXE FW itself is corrupted we need this strap.
GPIO_66	SIO_UART2_RTS_N	LPC boot BIOS strap	20K PD	1=boot from LPC; 0=do not boot from LPC (default) Note: The board should strap this low and do not use otherwise
GPIO_79	SIO_SPI_0_CLK	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_80	SIO_SPI_0_FS0	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_81	SIO_SPI_0_FS1	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_83	SIO_SPI_0_TXD	LPC 1.8V/3.3V mode select	20K PD	1=buffers set to 1.8V mode 0=buffers set to 3.3V mode (default)
GPIO_84	SIO_SPI_2_CLK	Allow SPI as a boot source	20K PU	1=disable 0=enable (default)
GPIO_85	SIO_SPI_2_FS0	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_86	SIO_SPI_2_FS1	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

GPIO #	Pin Name	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_175	AVS_M_DATA_2	eSPI vs. LPC	20K PD	1=eSPI mode; 0=LPC mode (default) Note: The default for A0 will be eSPI due to a bug on LPC.
GPIO_177	SMB_CLK	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_191	CNV_BRI_DT	eSPI Flash Sharing Mode	20K PD	eSPI Flash Sharing Mode: 1=slave attached flash sharing (SAFS); 0=master attached flash sharing (MAFS; default) Note: If eSPI mode is disabled (eSPI/LPC hard strap(GPIO_175) is set to select LPC) then the eSPI slave attached flash sharing strap must also be set to 0.
GPIO_192	CNV_BRI_RSP	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_193	CNV_RGI_DT	RSVD	20K PU	Ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_194	CNV_RGI_RSP	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_195	CNV_RF_RESET_N	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_196	XTAL_CLKREQ	RSVD	20K PD	Ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

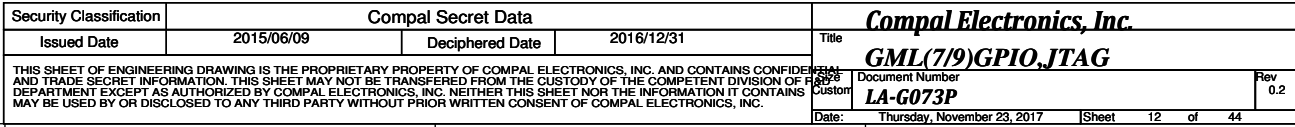


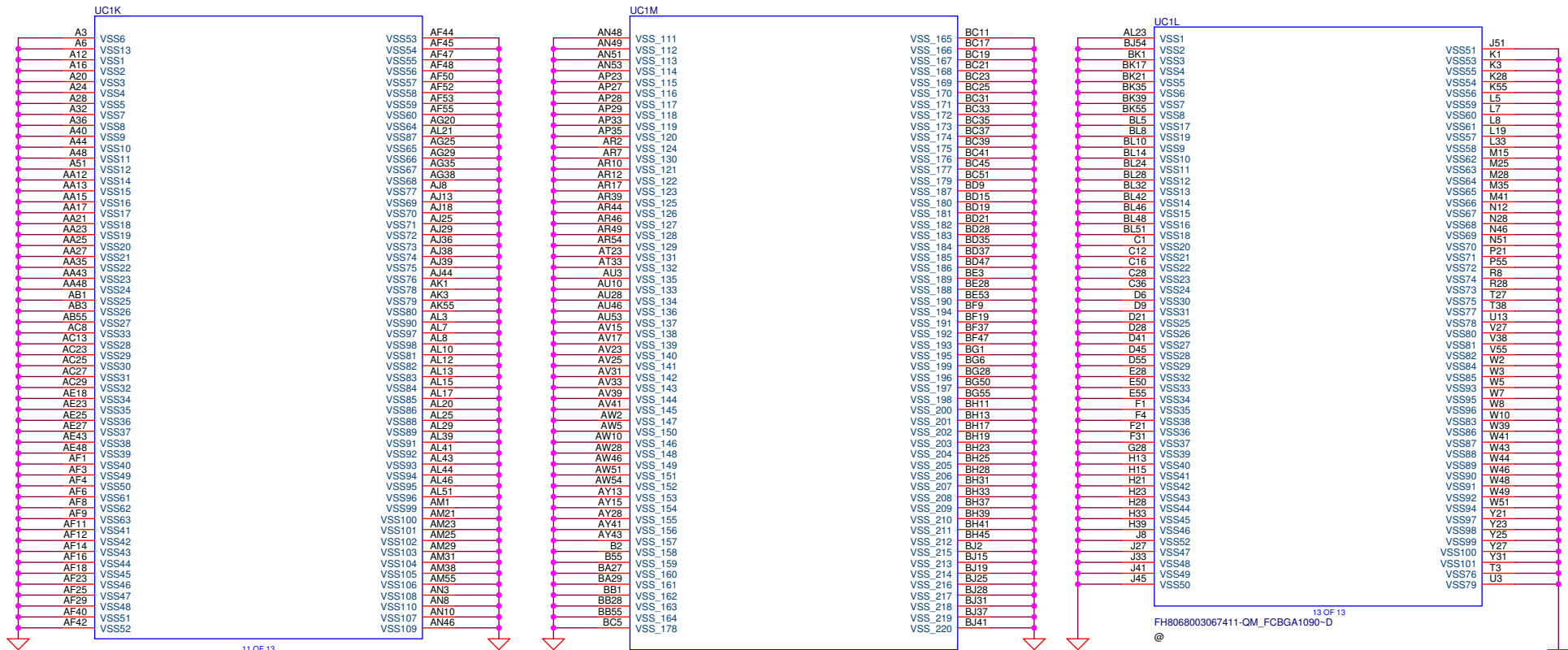
LPC 0= 3.3V(default), 1= 1.8V

SPI Boot Mode 1=disable 0=enable(default)



Security Classification	Compal Secret Data			Title	
Issued Date	2015/06/09	Deciphered Date	2016/12/31	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-G073P	0.2
				Date:	Thursday, November 23, 2017
				Sheet	11 of 44

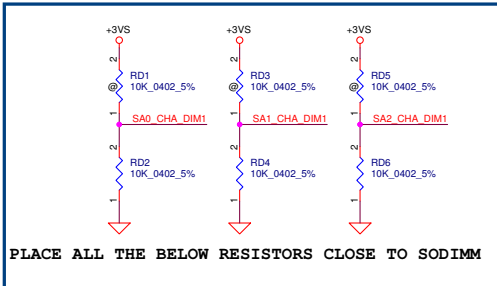




CHANNEL-A

REVERSE TYPE (5.2 mm)

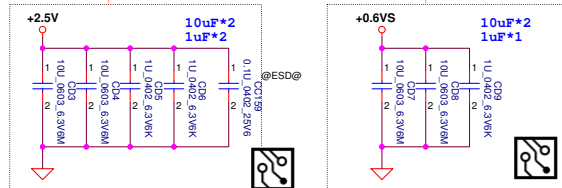
TOP: JDIMM1 CONN Non-ECC DIMM



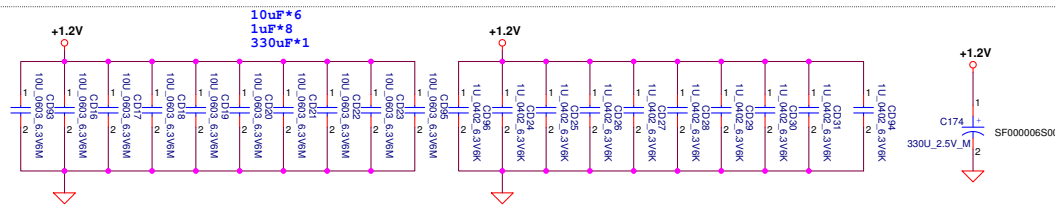
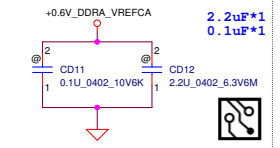
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM1.257,259

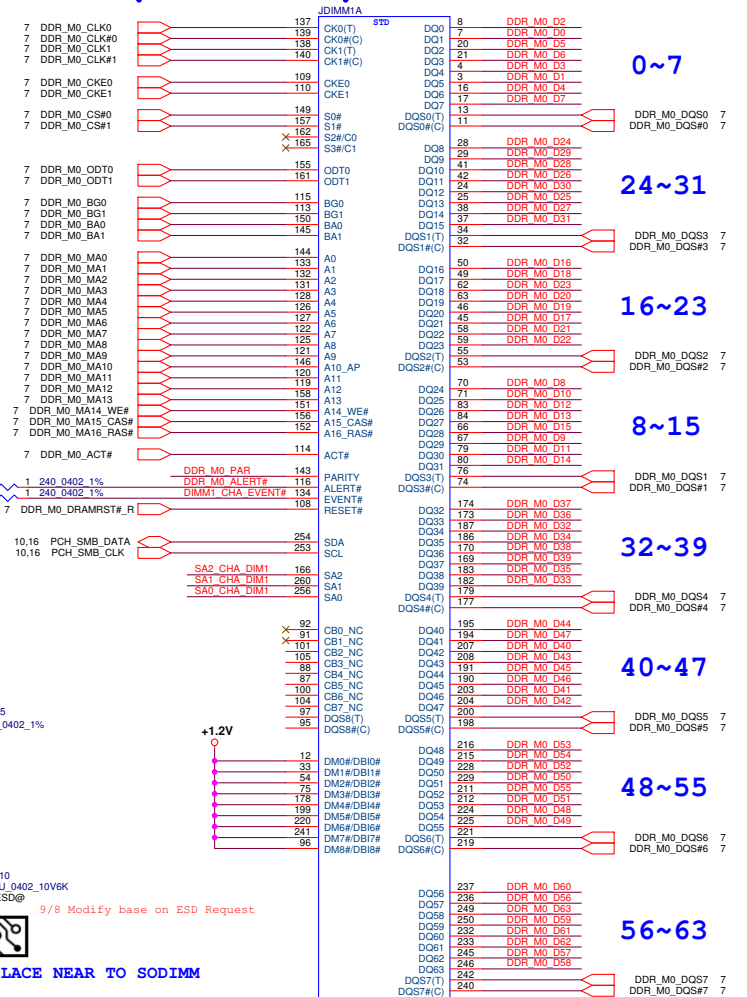
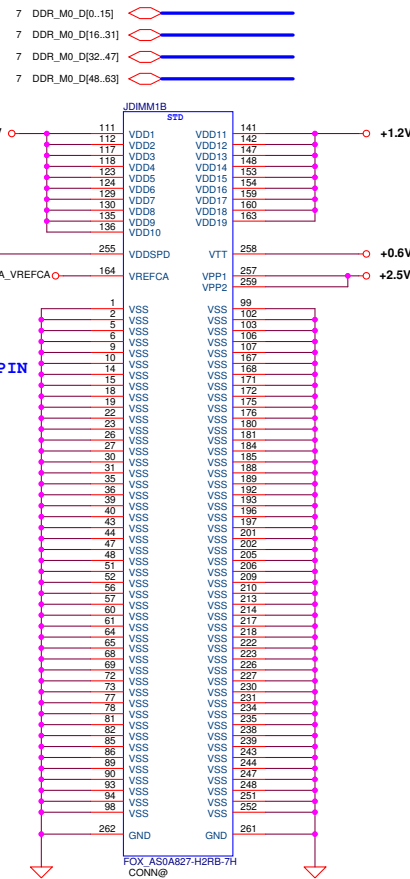
Layout Note:
Place near JDIMM1.258



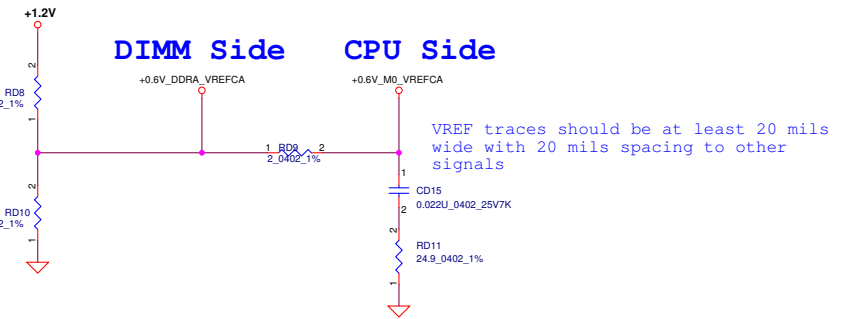
Layout Note:
PLACE THE CAP near JDIMM1. 164



Interleaved Memory



DIMM Side CPU Side



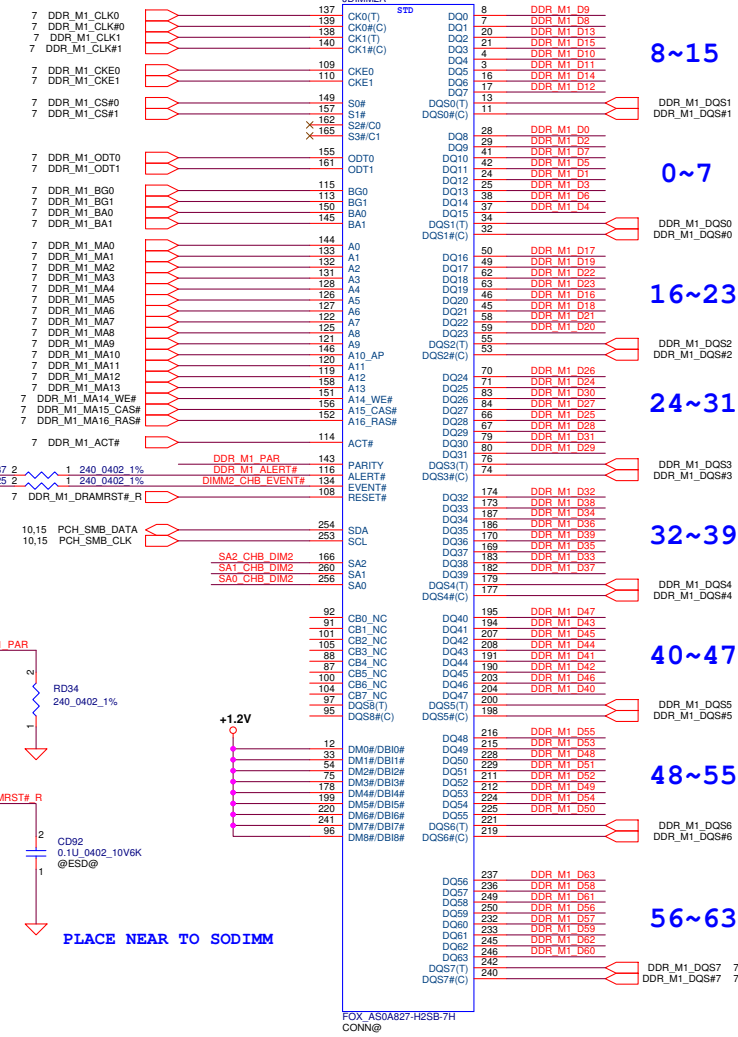
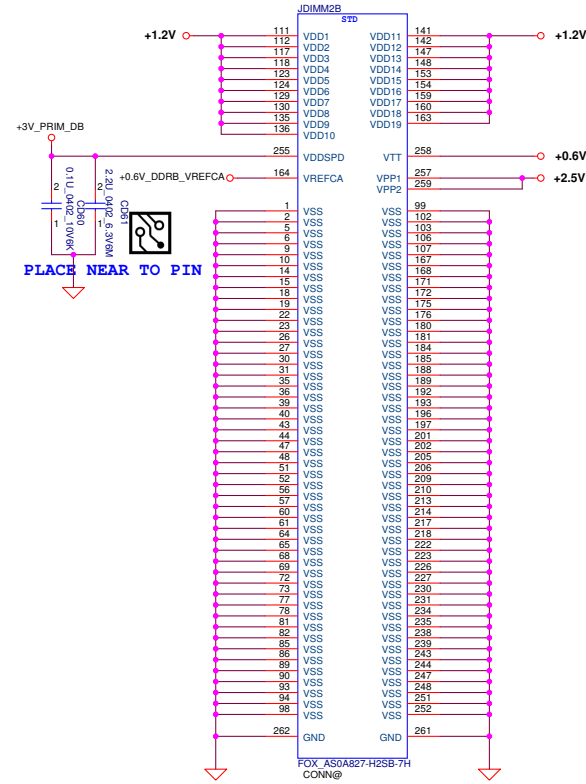
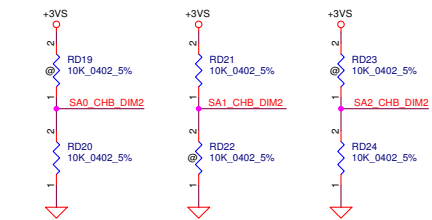
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/08/03	Deciphered Date	2015/12/31	Title	P18-DDRIV_CHA: DIMM0
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIRST DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-G073P
				Rev	v1.0
				Date	Thursday, November 23, 2017
				Sheet	15 of 55

CHANNEL-B

STD (5.2 mm)

TOP: JDIMM2 CONN Non-ECC DIMM

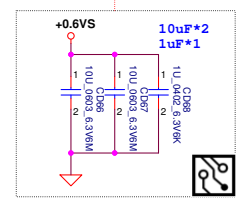
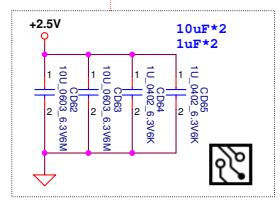
Interleaved Memory



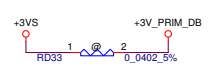
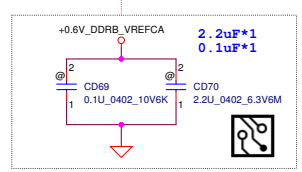
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM2.257,259

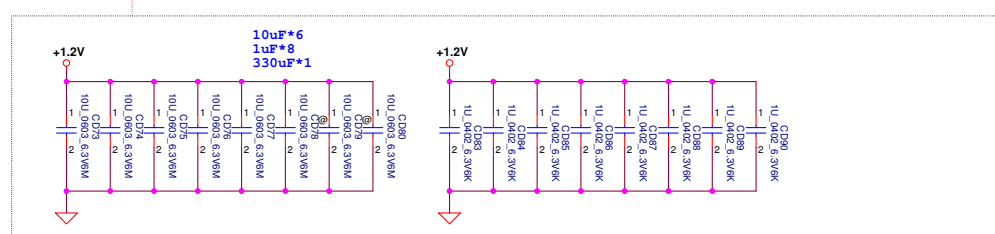
Layout Note:
Place near JDIMM2.258



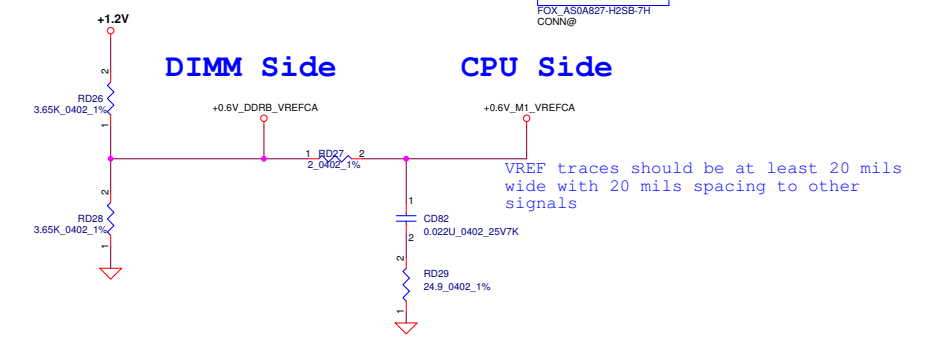
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM2

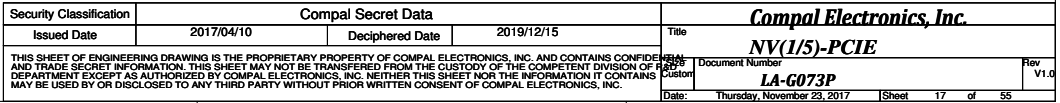


Layout Note:
Place near JDIMM2

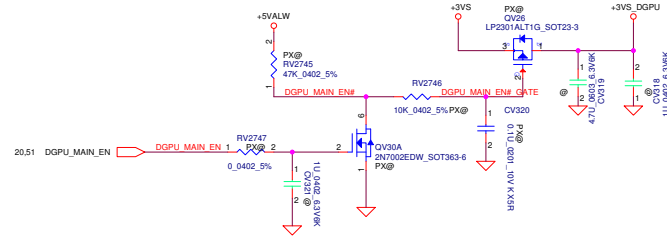


Part Number:LTCX0069FA0
Part Value:S SOCKET FOX AS0A827-H2SB-7H 260P DDR4





+3VS to +3VS_DGPU



+3VS to +3VS_DGPU_AON

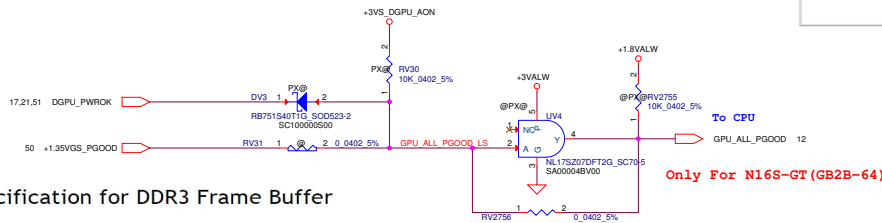
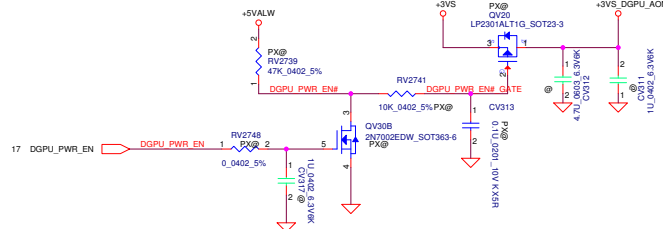


Table 3-7. Power Rail Specification for DDR3 Frame Buffer Interface

Constraint Parameter	Requirement
FBVDDQ/FBVDD	1.5 V (DDR3) or 1.35V (DDR3L)
DC tolerance	± 3%
AC tolerance	Transient noise tolerance: 80 mV pk-pk within 20 MHz BW High frequency noise tolerance: 200 mV pk-pk within 1 GHz BW

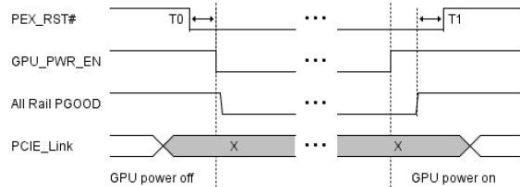


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

+1.0VALW to +1.0VS_DGPU

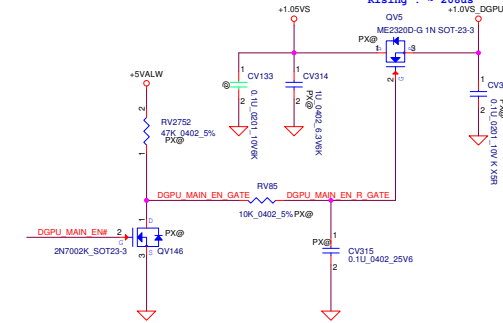


Table 5. EDP-Continuous³

Products	VRAM Type	GPU Core	GPU FBIO	FB Total ^{1,5}		1.05V Total ²	3.3V Total
		—	1.5V ⁴	1.35V ⁴	1.5V ⁴	1.35V ⁴	1.05V ⁴
		(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	19.0	—	2.0	—	4.2	0.80
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80
N16S-GTR	GDDR5	26.5	—	2.0	—	4.2	0.80
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80

Table 3-15. PCI Express Power Rails Specification

GPU Package	Power Rails	Voltage	Transient Noise
GB2-64/ GB2B-64	PEX_IOVDD/Q	1.05 V ± 30 mV	100 mV pk-pk within 20 MHz (1.05V)
	PEX_PLLVDD	1.0 V ± 15mV	70 mV pk-pk within 20 MHz (1.0V)

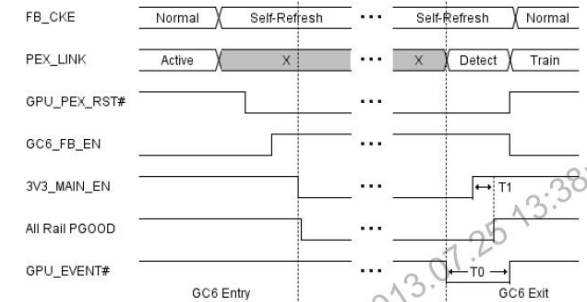


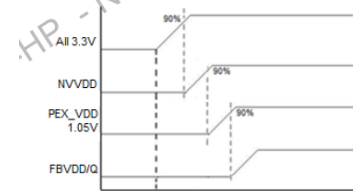
Figure 18-15. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-3. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Note:

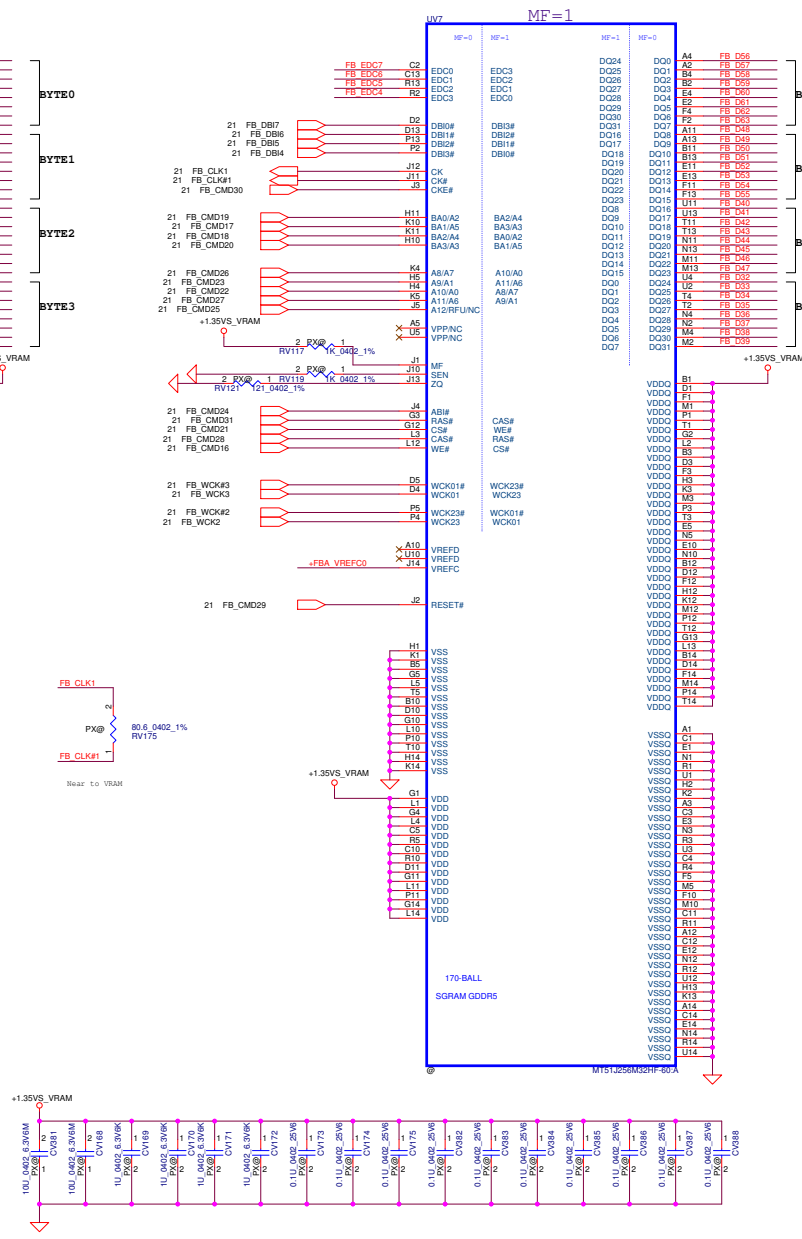
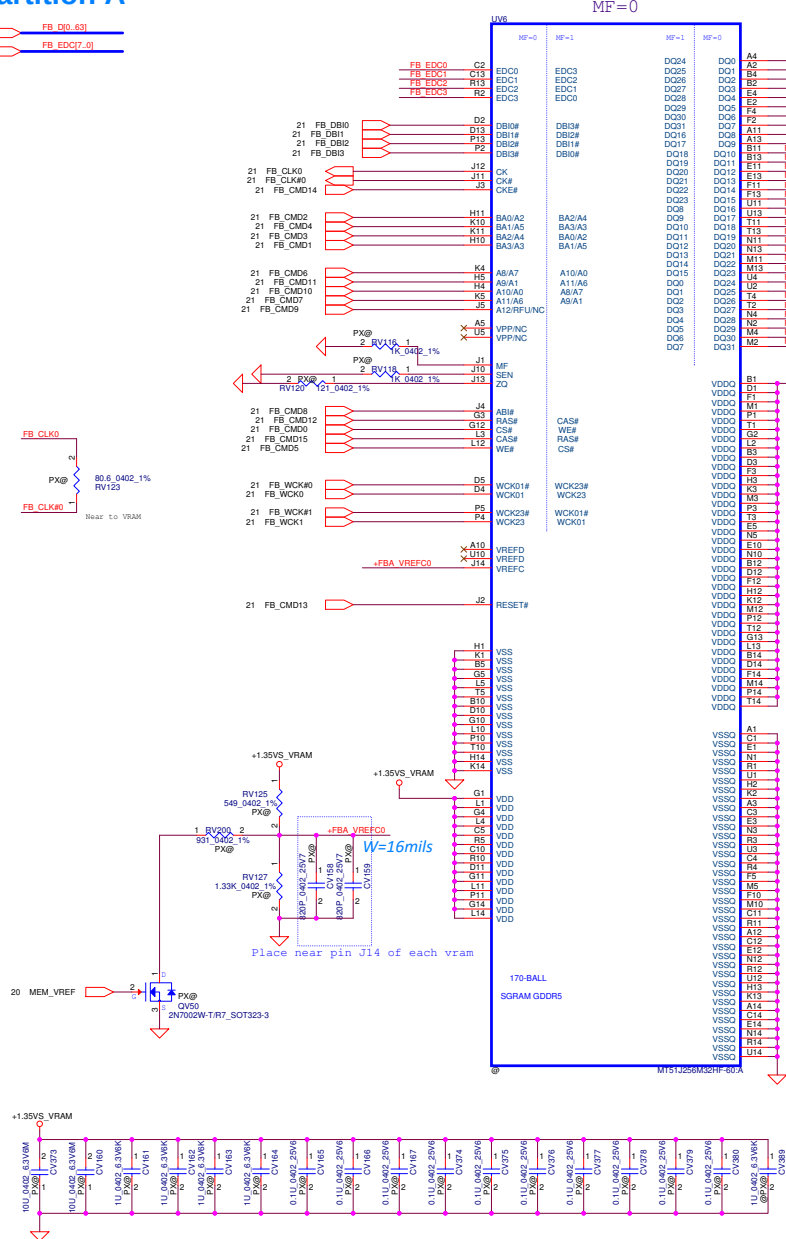
- The ramp time for any rail must be more than 40 μs and is recommended to be less than 2ms.



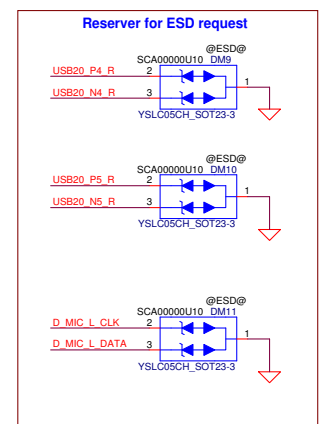
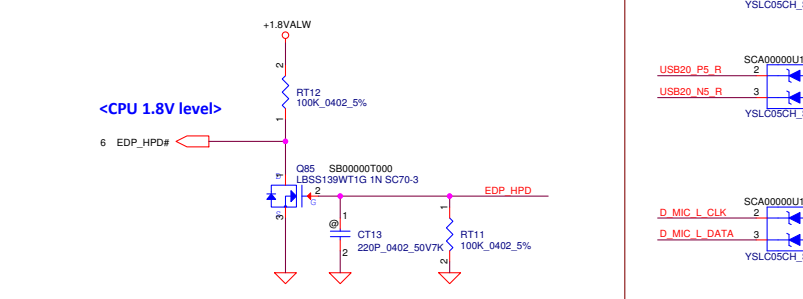
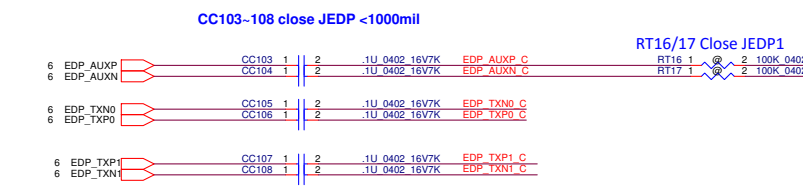
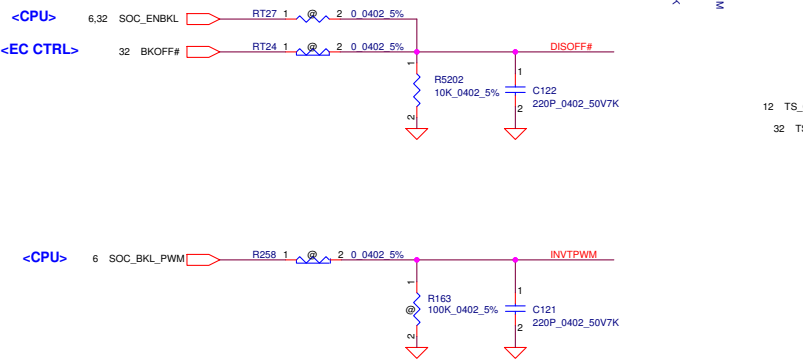
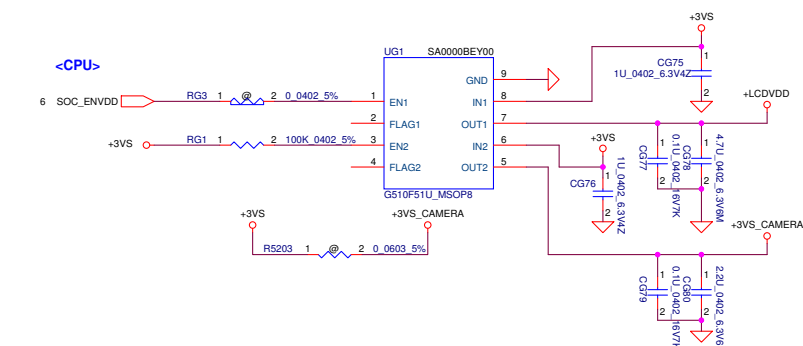
Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-7. Example of Power-Up Sequencing Order

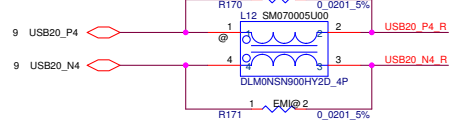
Memory Partition A



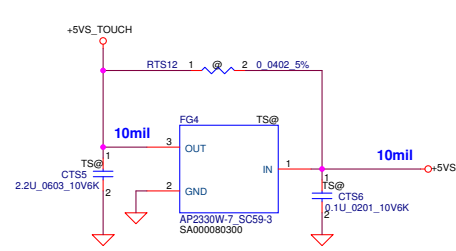
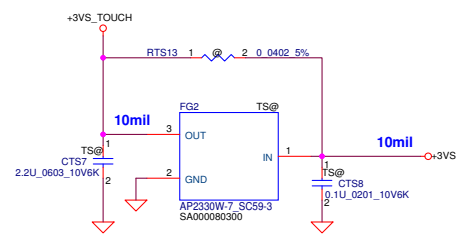
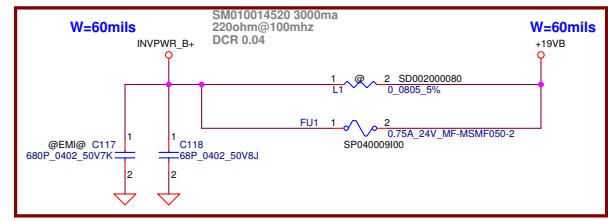
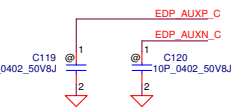
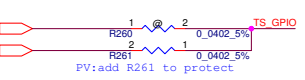
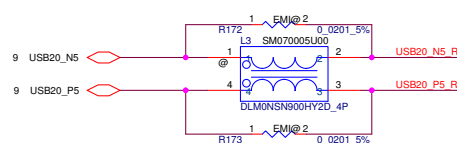
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/04/10	Deciphered Date	2019/12/15	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT BEING AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINED HEREIN MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			NIGP GDDR5 A Document Number LA-G073P	
Date	Issued	Approved	By	Rev
	2017/04/10	2017/04/10	2017/04/10	1.0



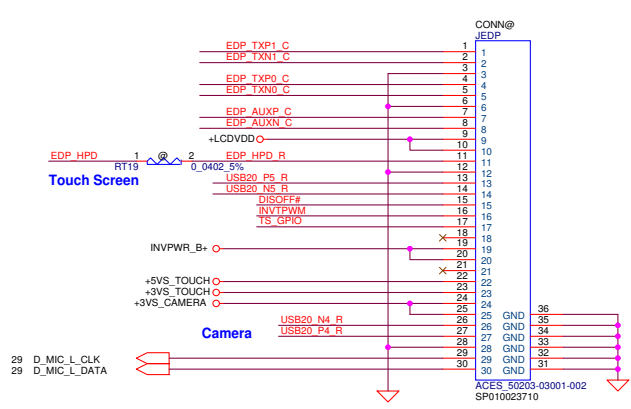
Camera



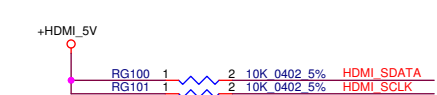
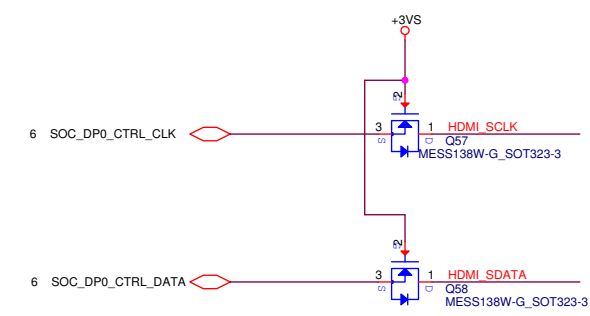
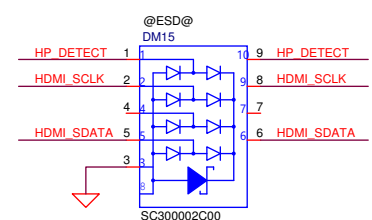
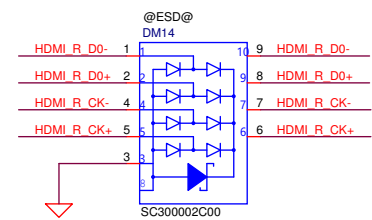
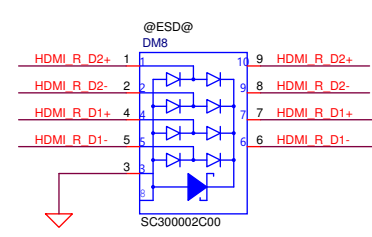
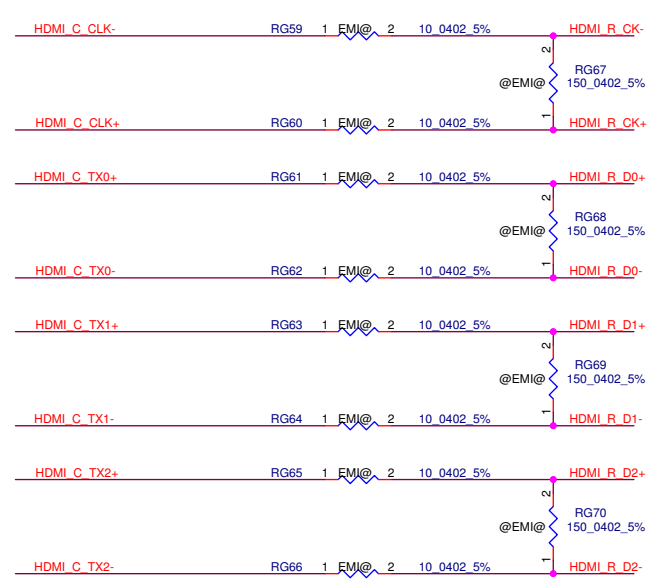
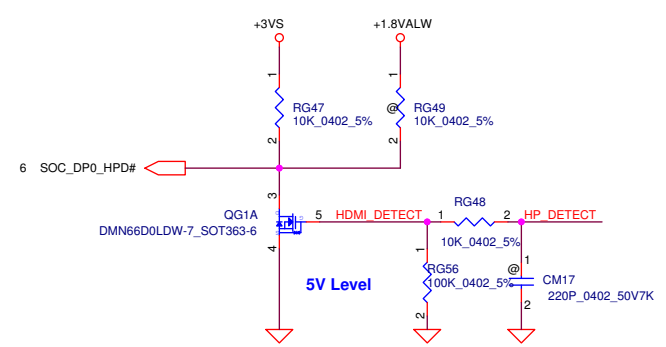
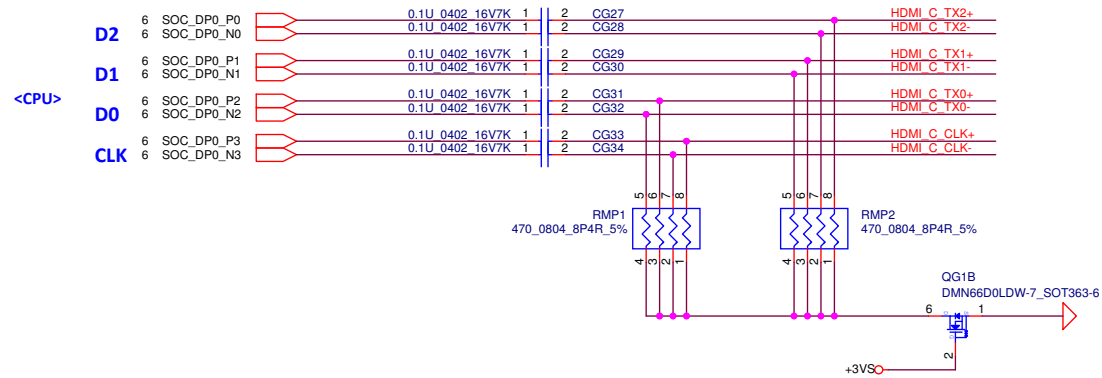
Touch Screen



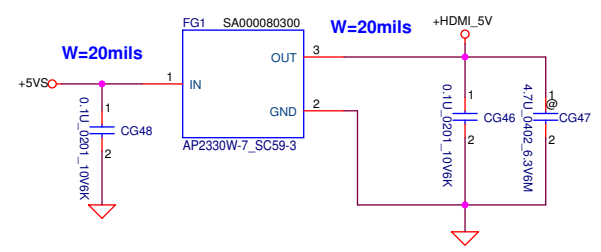
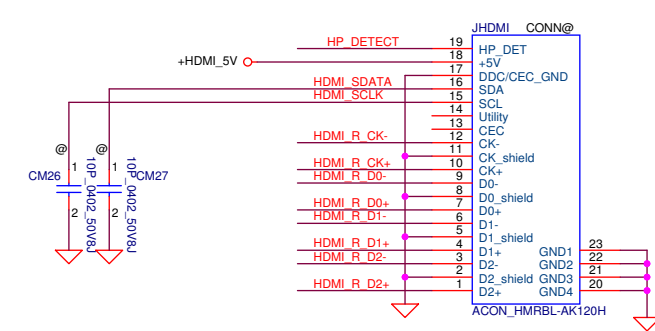
LCD/LED PANEL Conn.



Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		Document Number	
2017/07/10		2018/07/10		EDP Connector	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF ASST. DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Rev 1.0		Date: Thursday, November 23, 2017 Sheet 24 of 55	

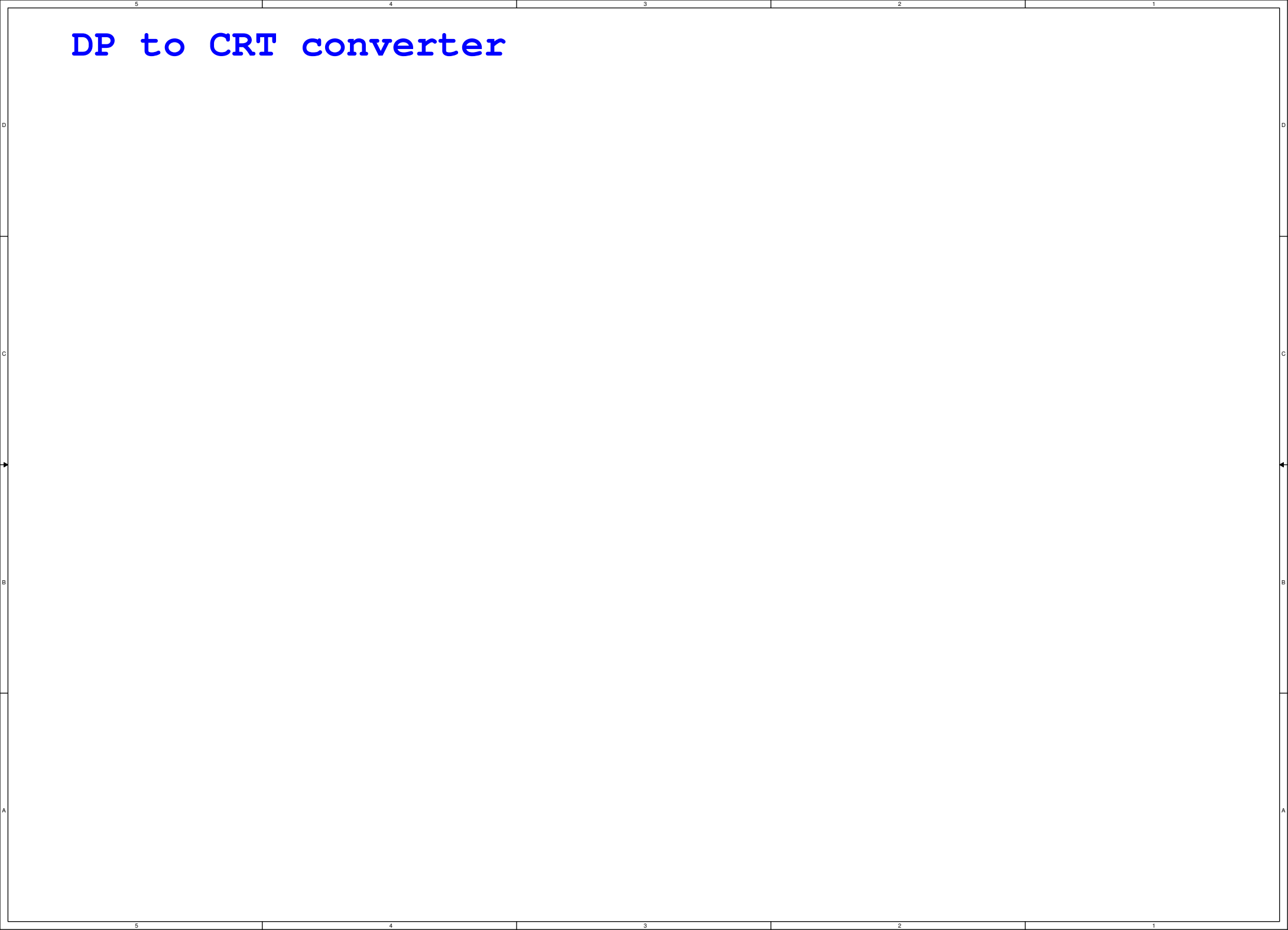


HDMI Conn.

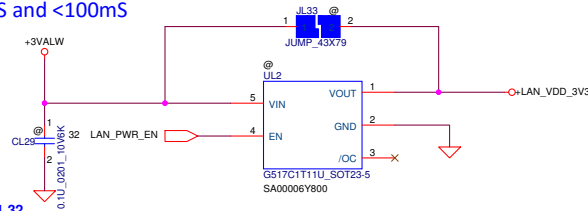


Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2017/07/10		Deciphered Date		2018/07/10		Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						HDMI Conn/Level shift					
						Document Number				Rev	
						LA-G073P				1.0	
						Date:		Thursday, November 23, 2017		Sheet 25 of 55	

DP to CRT converter



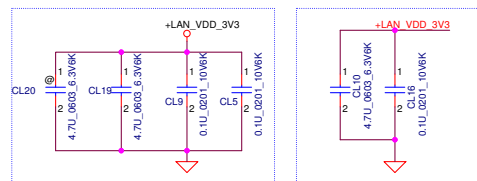
+LAN_VDD_3V3 Rising time
need>0.5mS and <100mS



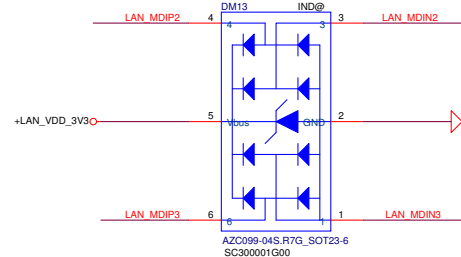
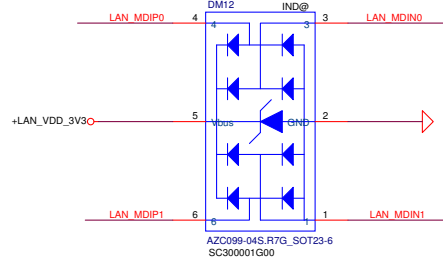
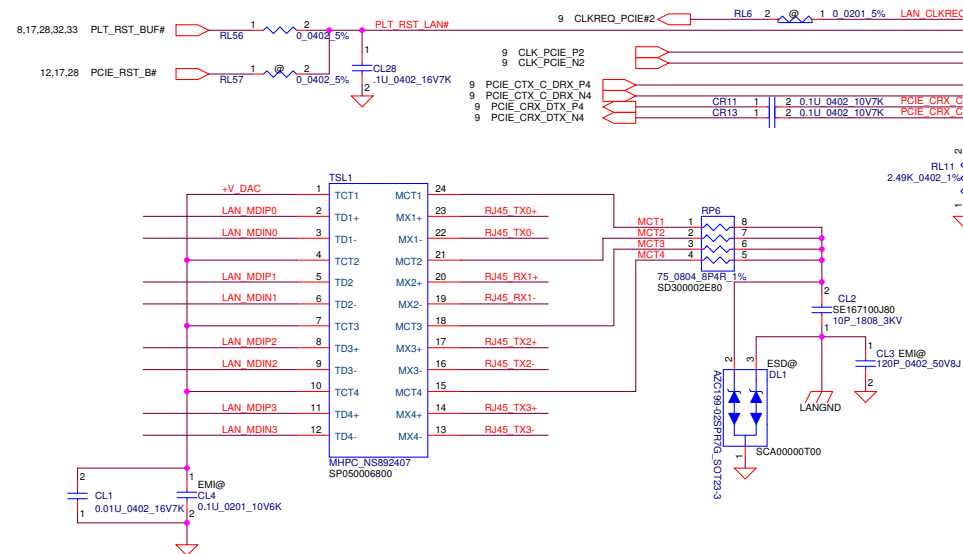
CL9 & CL5 close to UL1: Pin 11,32

CL19 close to UL1: Pin 32

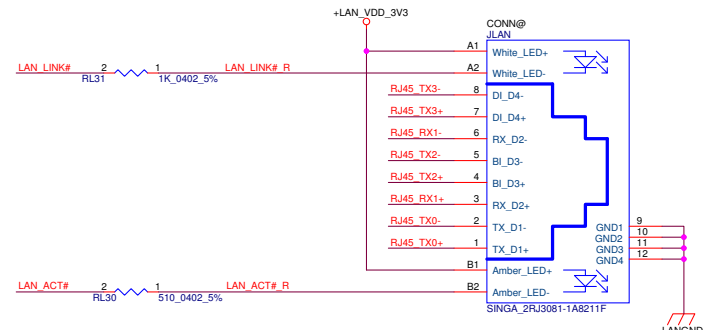
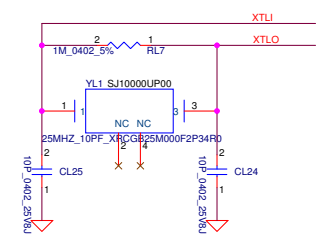
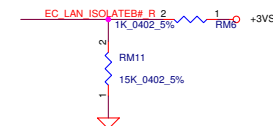
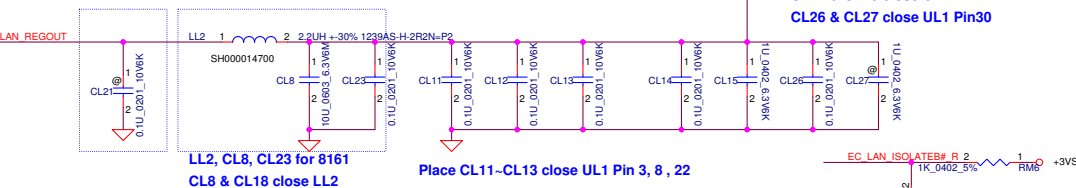
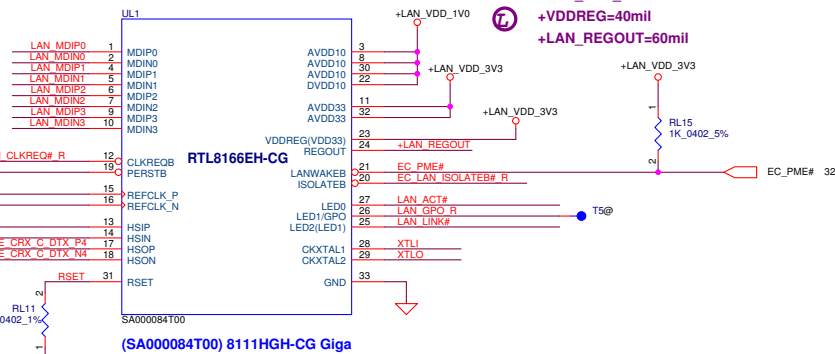
CL20 close to UL1: Pin 11



CL10 & CL16 close to UL1: Pin 23

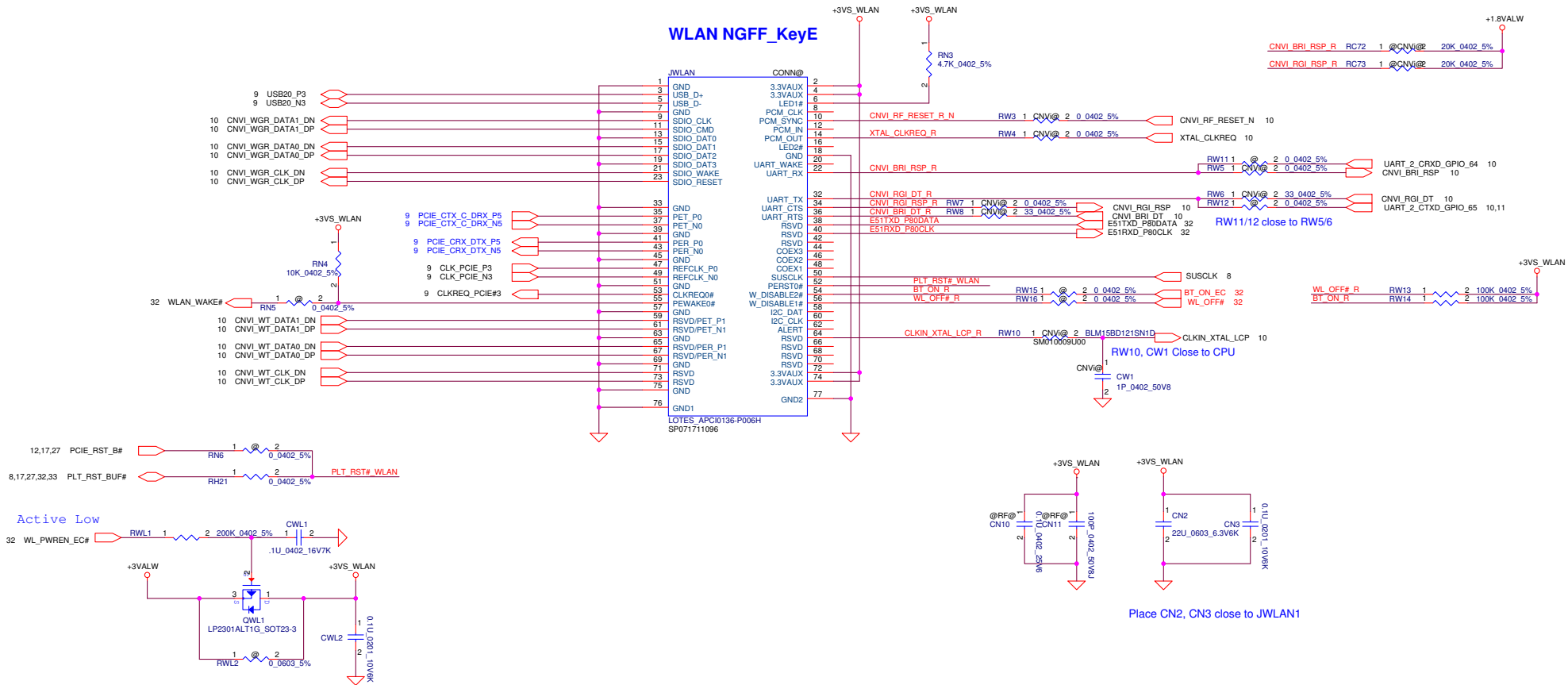


8111/8166 Co-Lay



Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		2018/07/10	
2017/07/10		2018/07/10		2018/07/10	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIRST DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Document Number		Rev 1.0	
LA-G073P		Thursday, November 23, 2017		Sheet 27 of 55	

WLAN NGFF_KeyE





Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/07/10	Deciphered Date	2018/07/10	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIRST INFORMATION TECHNOLOGY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				USB to SATA ASM1153	
				Document Number	Rev
				LA-G073P	1.0
Date:		Thursday, November 23, 2017		Sheet	30 of 55

MIPI-60 debug Conn.

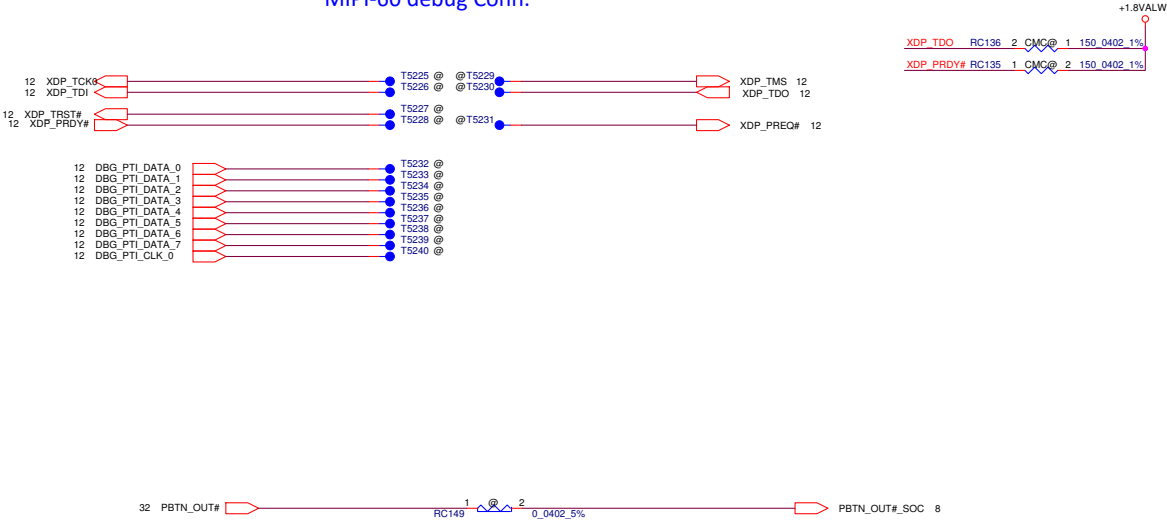
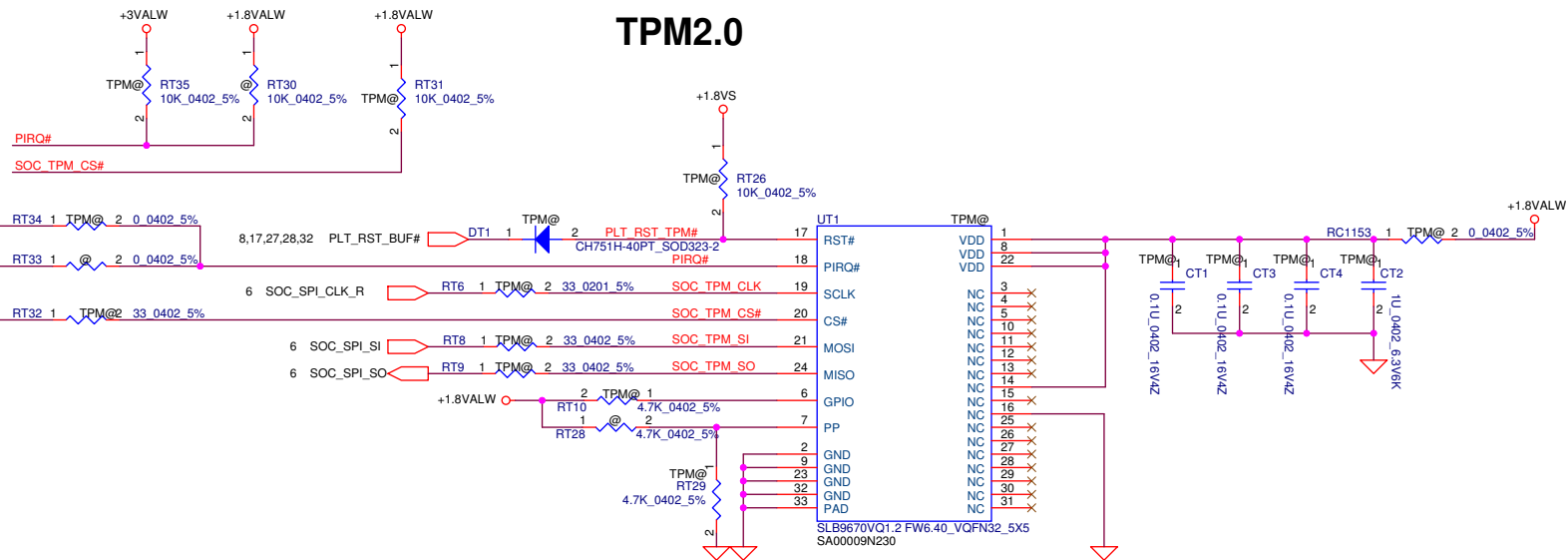
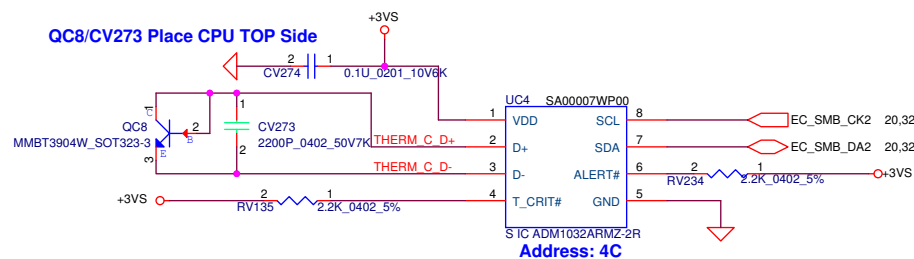


Table 167. MIPI-60 Connector Pinout

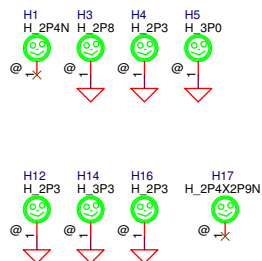
Pin	MIPI-60 Signal Name	Target Signal Name	I/O	Pin	MIPI-60 Signal Name	Target Signal Name	I/O
1	VREF_DEBUG	V1P8	NA	2	TMS/TMSC	JTAG_TMS	O
3	TCK	JTAG_TCK	O	4	TDO/EXTA	JTAG_TDO	I
5	TDI/EXTB	JTAG_TDI	O	6	nRESET	PMU_RSTBTN_N. Refer to Figure 171	O
7	RTCK/EXTC	PMU_PLTRST_N	I	8	TRST_PD	10kOhm Pull-Down to GND	NA
9	nTRST/EXTD	JTAG_TRST_N	O	10	EXTF/TRIGIN	JTAG_PREQ_N	O
11	EXTF/TRIGOUT	JTAG_PRODY_N	I	12	VREF_TRACE	V1P8	NA
13	TRC_CLK0	GPIO_0	I	14	TRC_CLK1	GPIO_18 ¹	I
15	Target Presence Detect	Strapping resistor of SIO_SPI_2_TXD/ GPIO_123 Refer to Figure 220	NA	16	GND	GND	NA
17	TRC_DATA0[0]	GND	NA	18	TRC_DATA1[0]/ TRC_DATA0[20]	GPIO_19 ¹	I
19	TRC_DATA0[1]	GPIO_1	I/O	20	TRC_DATA1[1]/ TRC_DATA0[21]	GPIO_20 ¹	I
21	TRC_DATA0[2]	GPIO_2	I/O	22	TRC_DATA1[2]/ TRC_DATA0[22]	GPIO_21 ¹	I
23	TRC_DATA0[3]	GPIO_3	I/O	24	TRC_DATA1[3]/ TRC_DATA0[23]	GPIO_22 ¹	I
25	TRC_DATA0[4]	GPIO_4	I/O	26	TRC_DATA1[4]/ TRC_DATA0[24]	GPIO_23 ¹	I
27	TRC_DATA0[5]	GPIO_5	I/O	28	TRC_DATA1[5]/ TRC_DATA0[25]	GPIO_24 ¹	I
29	TRC_DATA0[6]	GPIO_6	I/O	30	TRC_DATA1[6]/ TRC_DATA0[26]	GPIO_25 ¹	I
31	TRC_DATA0[7]	GPIO_7	I/O	32	TRC_DATA1[7]/ TRC_DATA0[27]	GPIO_26 ¹	I
33	TRC_DATA0[8]	GPIO_8	I/O	34	TRC_DATA1[8]/ TRC_DATA0[28]	Connect to Pin 6 (RESET_BTN_N)	O
35	TRC_DATA0[9]	GPIO_10	I/O	36	TRC_DATA1[9]/ TRC_DATA0[29]	Strapping resistor of GP_SSP_0_FS1/ GPIO_106 (BOOT_HALT_N Strap) Refer to Figure 220	O
37	TRC_DATA3[0]/ TRC_DATA0[10]	GPIO_11	I/O	38	TRC_DATA2[0]/ TRC_DATA1[10]/ TRC_DATA0[30]	Connect to Pin 7 (PMU_PLTRST_N)	I
39	TRC_DATA3[1]/ TRC_DATA0[11]	GPIO_12	I/O	40	TRC_DATA2[1]/ TRC_DATA1[11]/ TRC_DATA0[31]	POWER_BTN_N	O
41	TRC_DATA3[2]/ TRC_DATA0[12]	GPIO_13	I/O	42	TRC_DATA2[2]/ TRC_DATA1[12]/ TRC_DATA0[32]	RSMRST_N	I
43	TRC_DATA3[3]/ TRC_DATA0[13]	GPIO_14	I/O	44	TRC_DATA2[3]/ TRC_DATA1[13]/ TRC_DATA0[33]	GPIO_28 ¹	I
45	TRC_DATA3[4]/ TRC_DATA0[14]	GPIO_15	I/O	46	TRC_DATA2[4]/ TRC_DATA1[14]/ TRC_DATA0[34]	GPIO_29 ¹	I
47	TRC_DATA3[5]/ TRC_DATA0[15]	GPIO_16	I/O	48	TRC_DATA2[5]/ TRC_DATA1[15]/ TRC_DATA0[35]	I2C_SCL	I/O
49	TRC_DATA3[6]/ TRC_DATA0[16]	GPIO_17	I/O	50	TRC_DATA2[6]/ TRC_DATA1[16]/ TRC_DATA0[36]	I2C_SDA	I/O
51	TRC_DATA3[7]/ TRC_DATA0[17]	No Connect	NA	52	TRC_DATA2[7]/ TRC_DATA1[17]/ TRC_DATA0[37]	GPIO_30 ¹	I
53	TRC_DATA3[8]/ TRC_DATA0[18]	No Connect	NA	54	TRC_DATA2[8]/ TRC_DATA1[18]/ TRC_DATA0[38]	UART1_TXD/GPIO_43	I
55	TRC_DATA3[9]/ TRC_DATA0[19]	No Connect	NA	56	TRC_DATA2[9]/ TRC_DATA1[19]/ TRC_DATA0[39]	UART1_RXD/GPIO_42	O
57	GND	GND	NA	58	GND	GND	NA
59	TRC_CLK3	GPIO_9	I	60	TRC_CLK2	GPIO_27 ¹	I



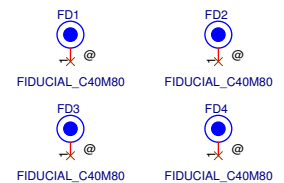
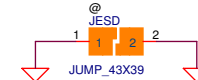
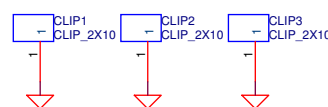
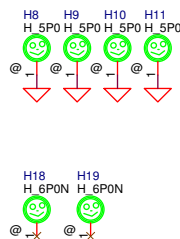
CPU Thermal Sensor



GPU

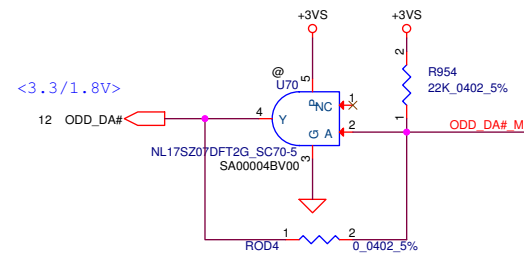
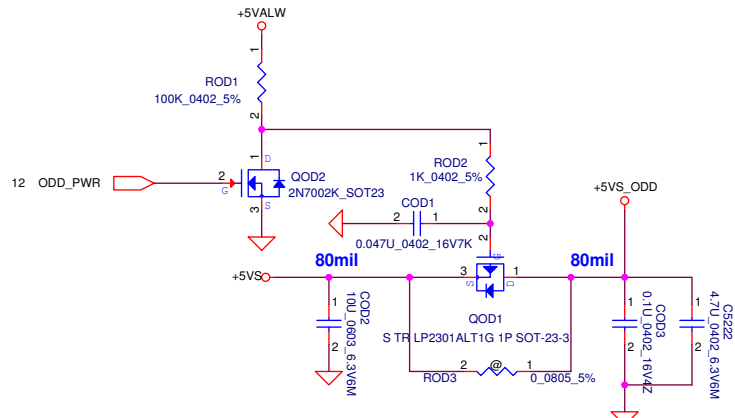
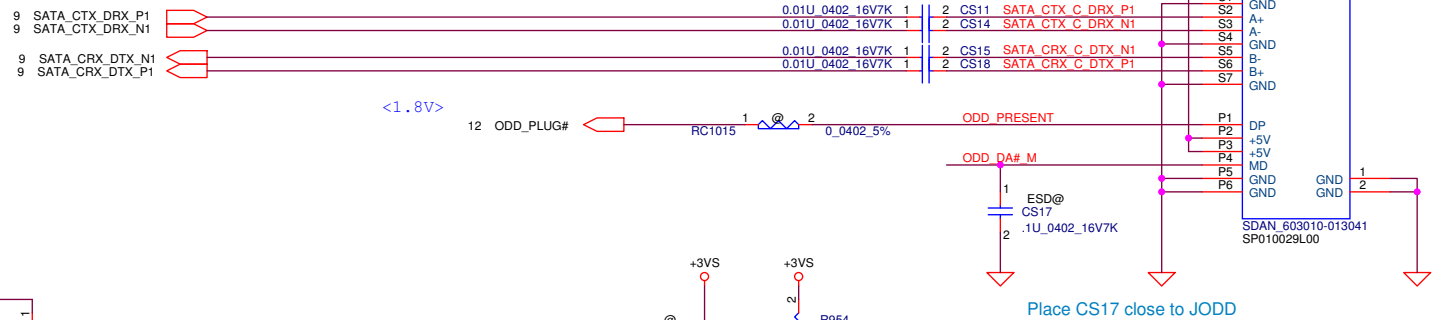


CPU



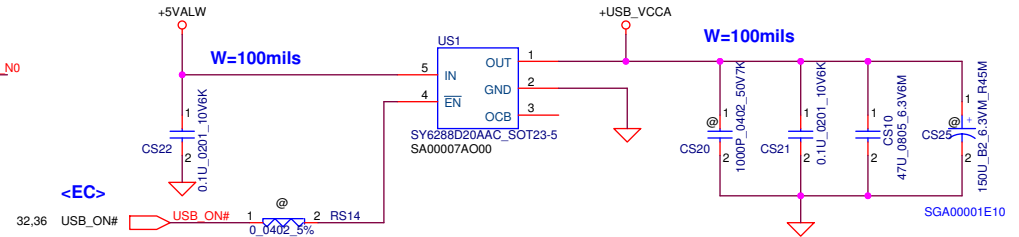
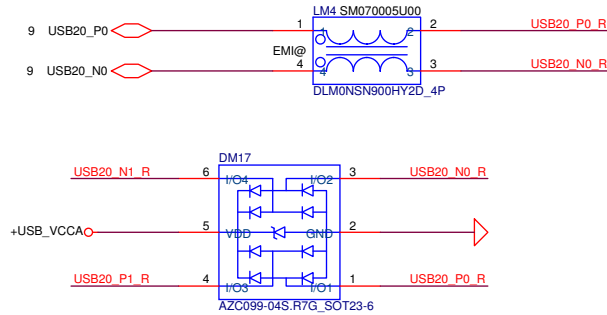
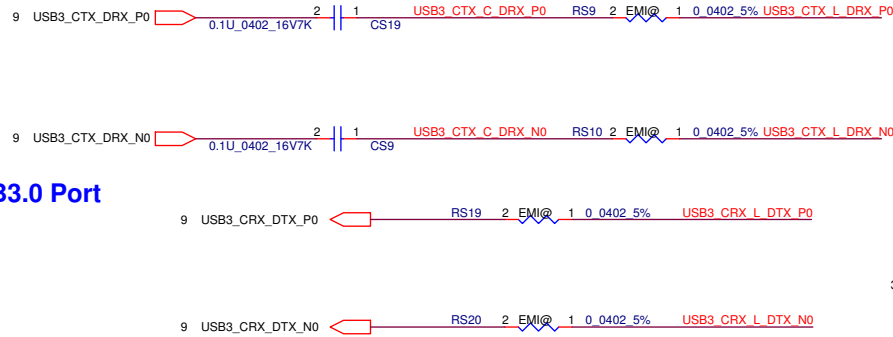
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date		2017/07/10	Deciphered Date	2018/07/10	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					TPM/Thermal/Screw hole		
					Document Number		
					LA-G073P		
					Date:	Thursday, November 23, 2017	Sheet 33 of 55
					Rev 1.0		

2.5" SATA HDD connector

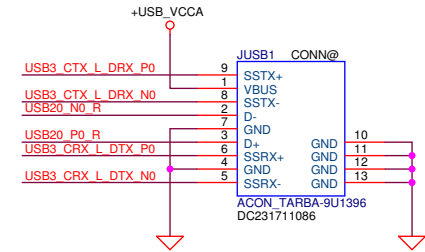


Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2017/07/10	Deciphered Date	2018/07/10	Title	ODD/SATA Conn		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FACTORY DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Part Number	Document Number	Rev	
				Customer	LA-G073P	1.0	
				Date:	Thursday, November 23, 2017	Sheet 34 of 55	

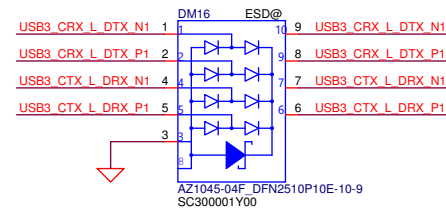
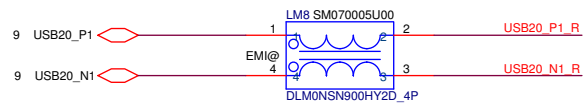
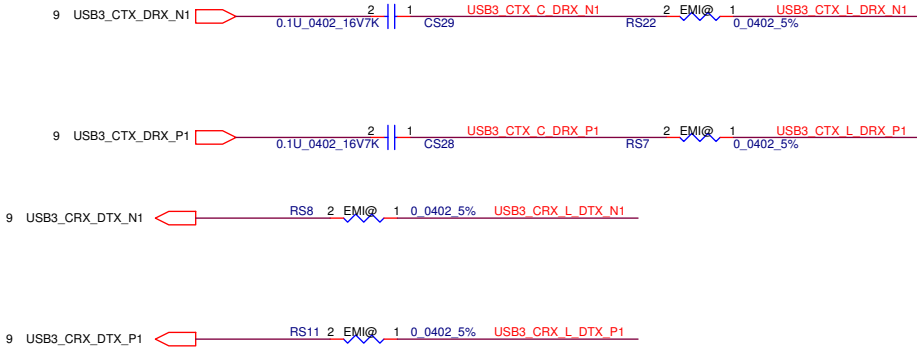
USB3.0 Port



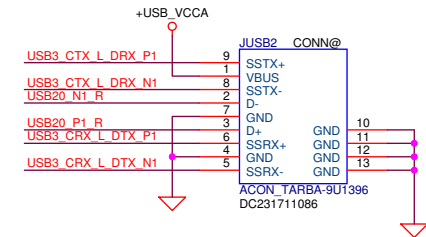
USB2.0/USB3.0 port



USB3.0 Port

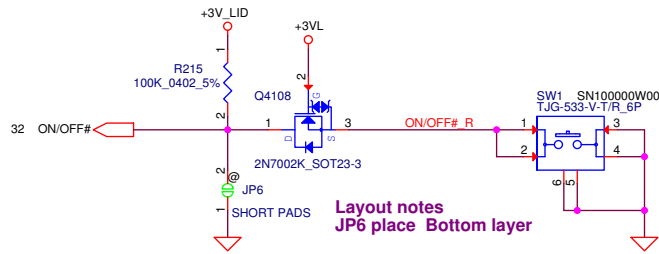


USB2.0/USB3.0 port 1

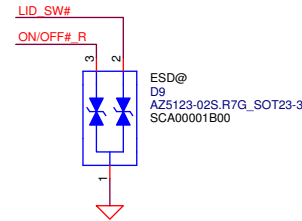


Security Classification		Compal Secret Data		Compal Electronics, Inc.					
Issued Date		2017/07/10		Deciphered Date		2018/07/10		Title	
								USB 3.0/2.0 conn	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						Part Number		Rev	
						Docu		1.0	
						Custom			
						LA-G073P			
						Date:		Thursday, November 23, 2017	

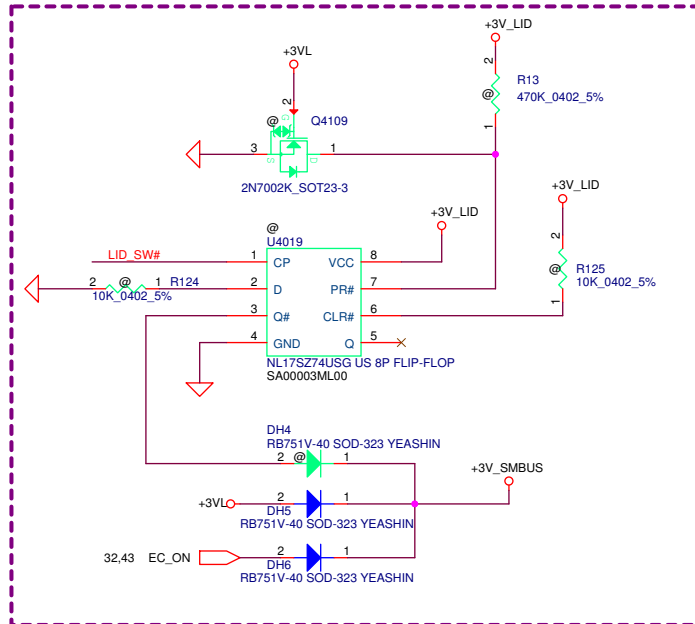
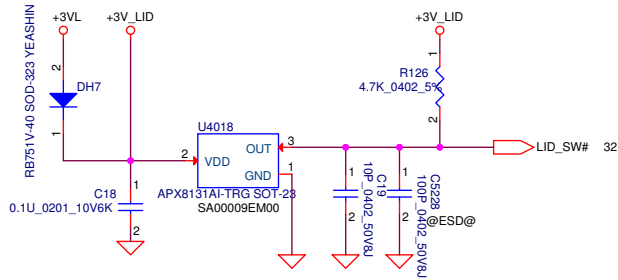
Power Button Switch



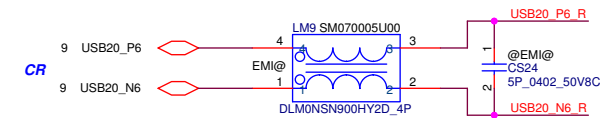
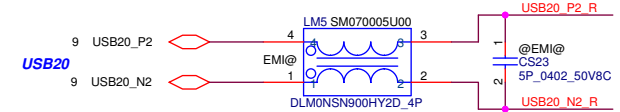
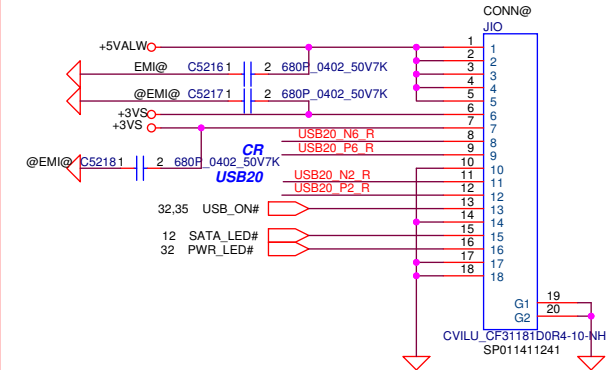
ESD Diode



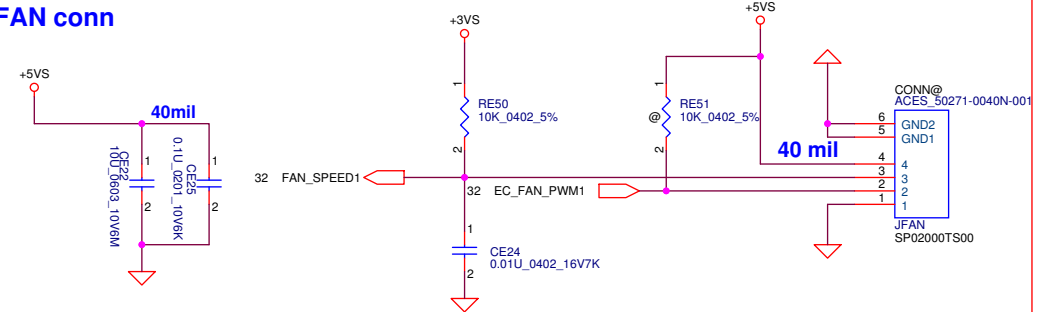
Lid Switch (Hall Effect Sensor)



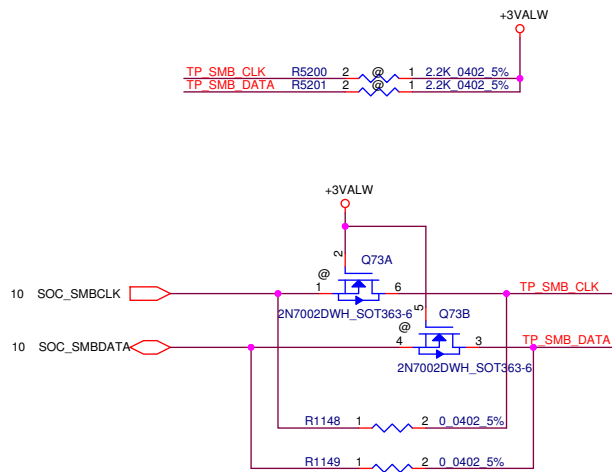
JIO S/B



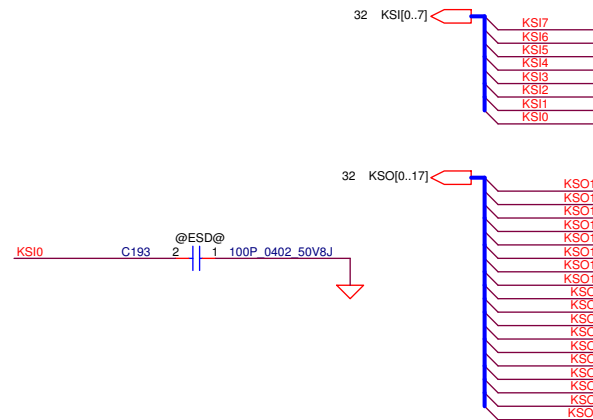
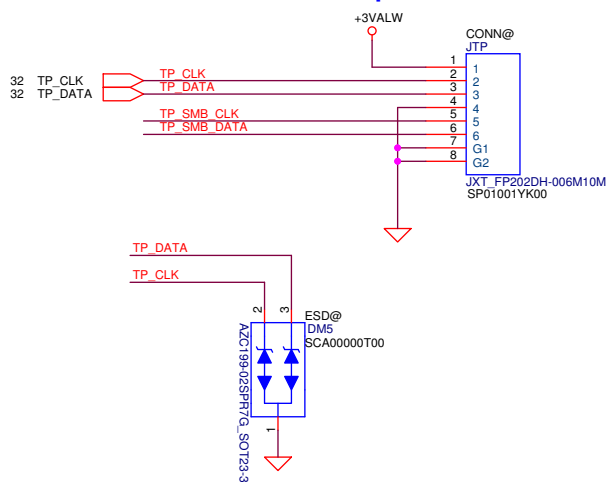
FAN conn



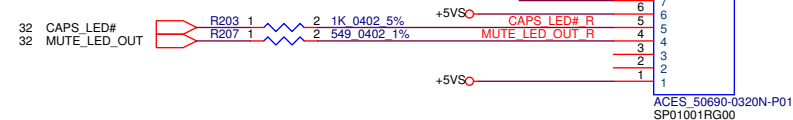
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2017/07/10	Deciphered Date	2018/07/10	Title	PWRBTN/FAN/IO	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Part Number	Rev	
				Customer	1.0	
				LA-G073P		
				Date:	Thursday, November 23, 2017	Sheet



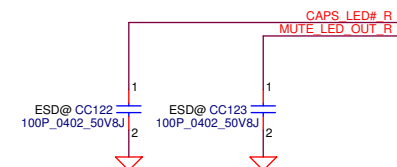
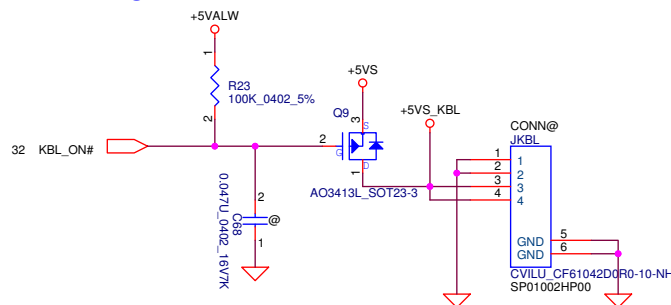
Touch pad conn



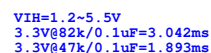
Keyboard conn



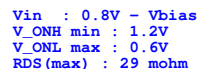
KB backlight Conn



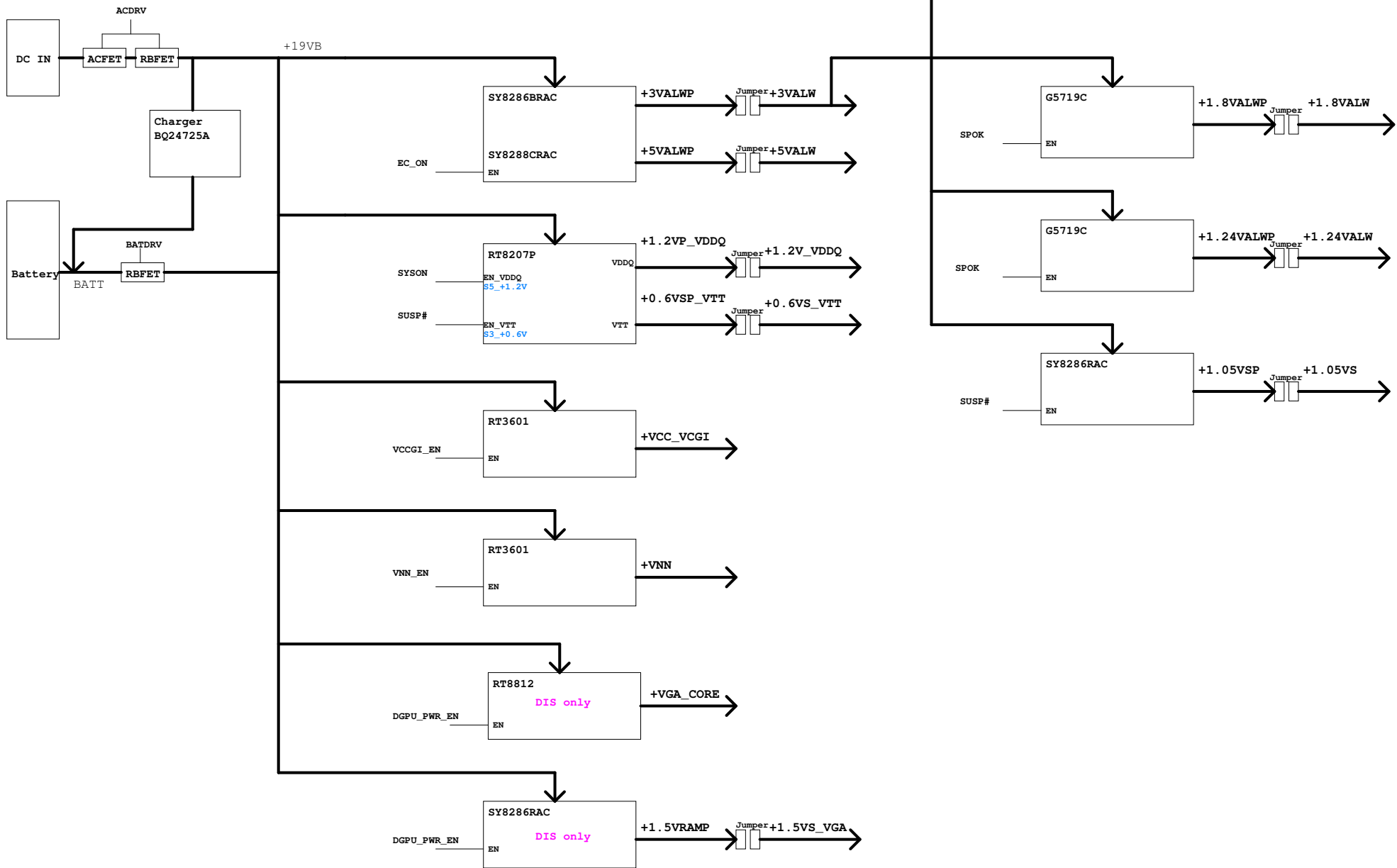
I (Max) : 0.2 A(Codec)
RDS(max) : 150 mohm
V drop : 0.03V



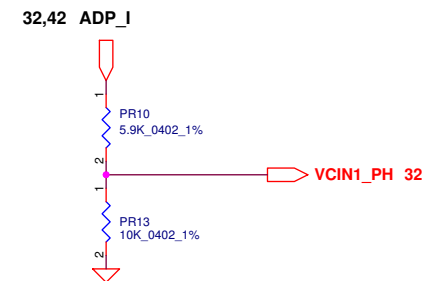
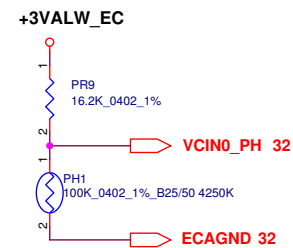
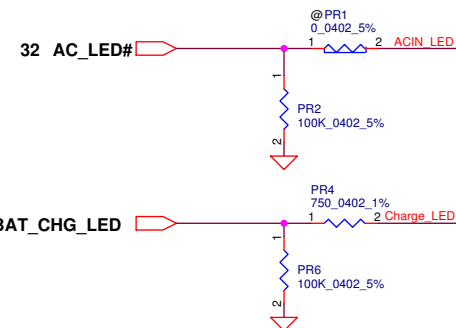
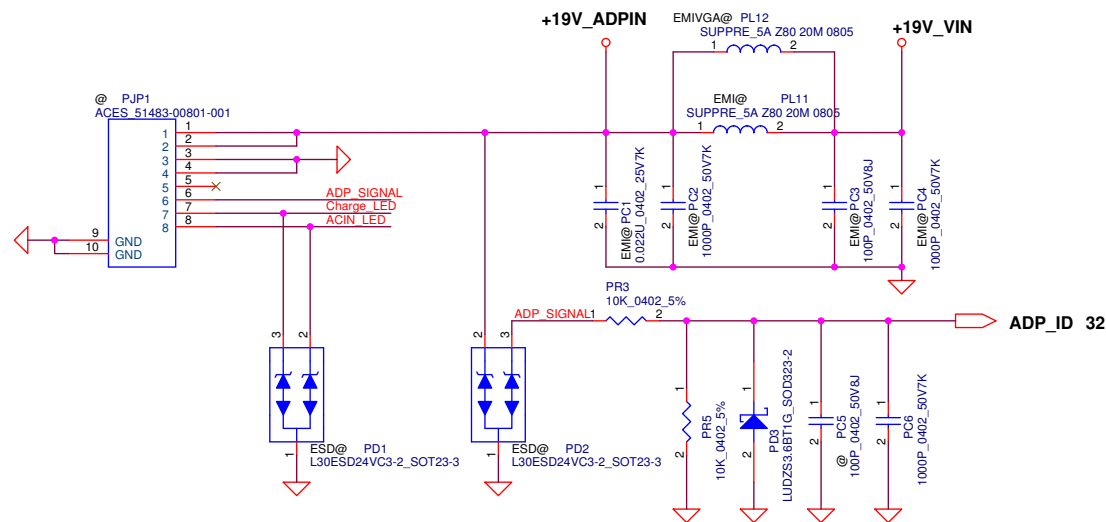
VIH=1.2~5.5V
3.3V@100k/0.1uF=3.538ms
3.3V@120k/0.1uF=4.272ms



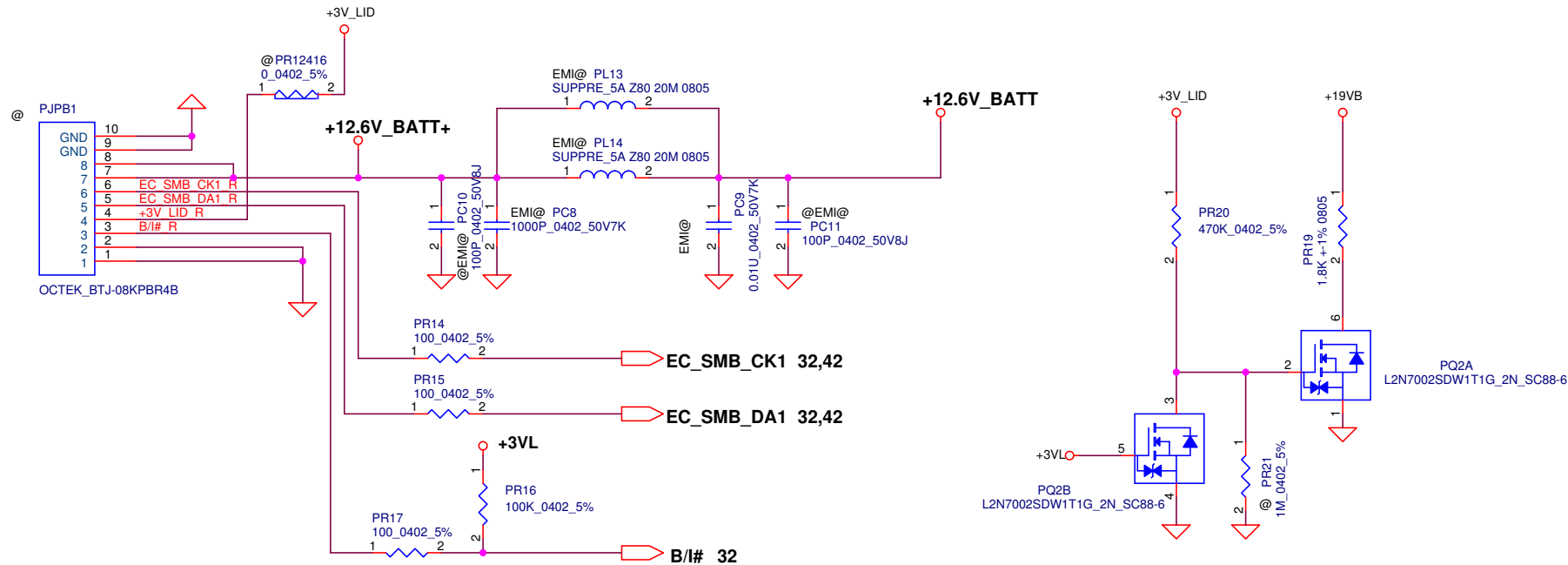
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/07/10	Deciphered Date	2018/07/10	Title	DC Interface
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Part Number Custom	Rev 1.0
Date: Thursday, November 23, 2017				Sheet 38 of 55	



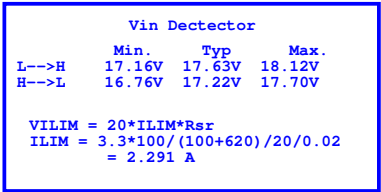
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/09/01	Deciphered Date	2018/09/01	Title	Power Block Diagram
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIRST DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				Intel / Gemini Lake	0.1
				Date:	Thursday, November 23, 2017
				Sheet	39 of 53



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/09/01	Deciphered Date	2018/09/01	Title	DC Conn
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Intel / Gemini Lake
				Date:	Thursday, November 23, 2017
				Sheet	40 of 53
				Rev	0.1

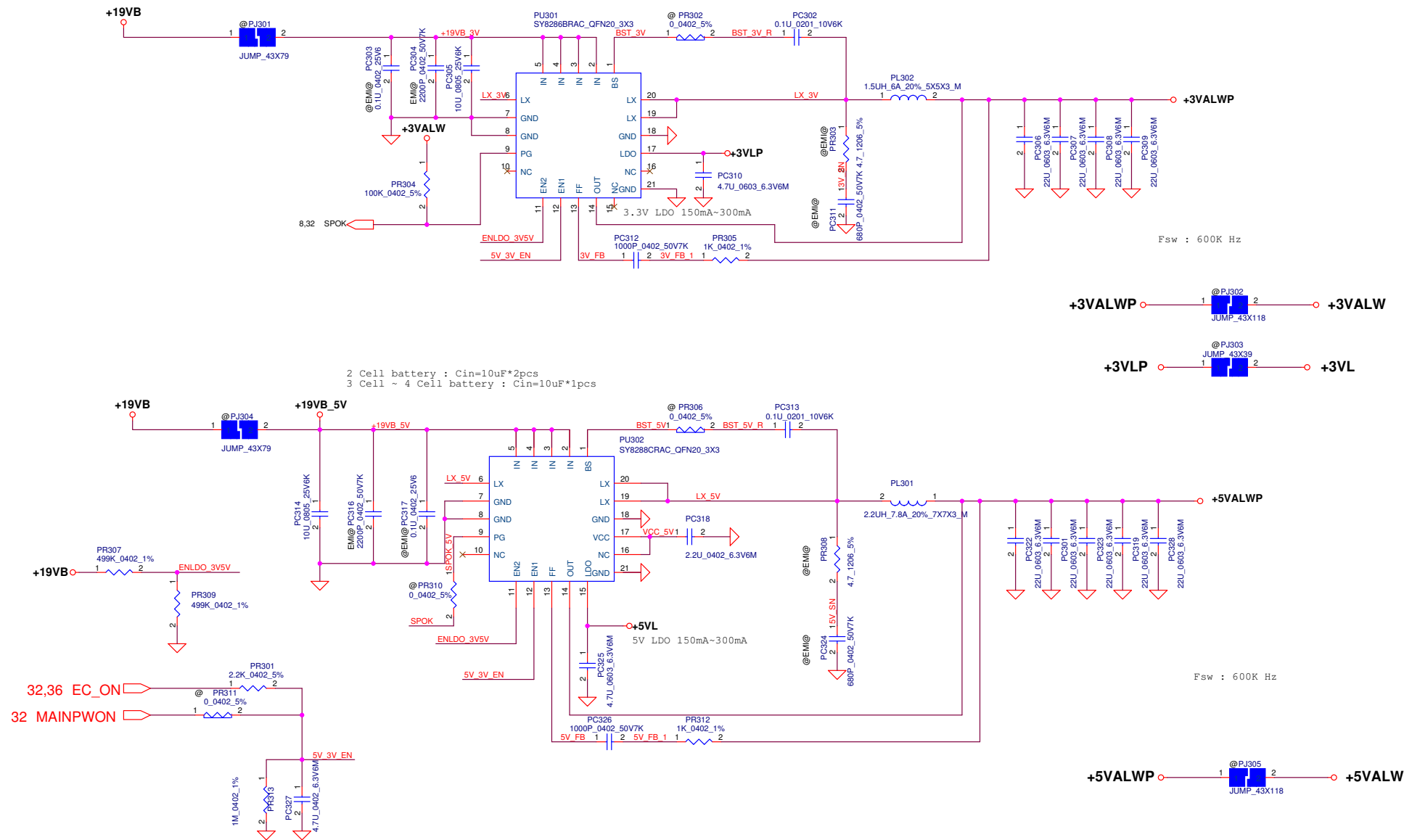


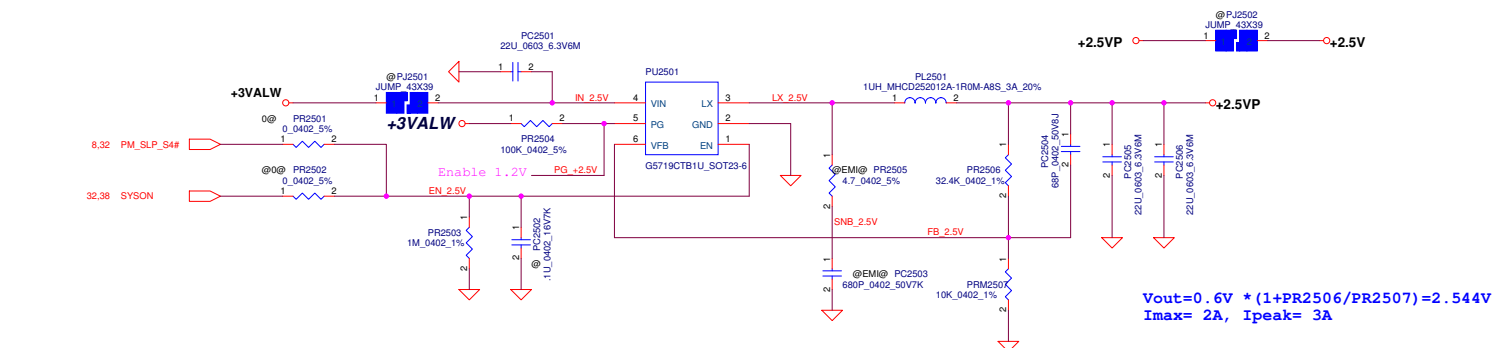
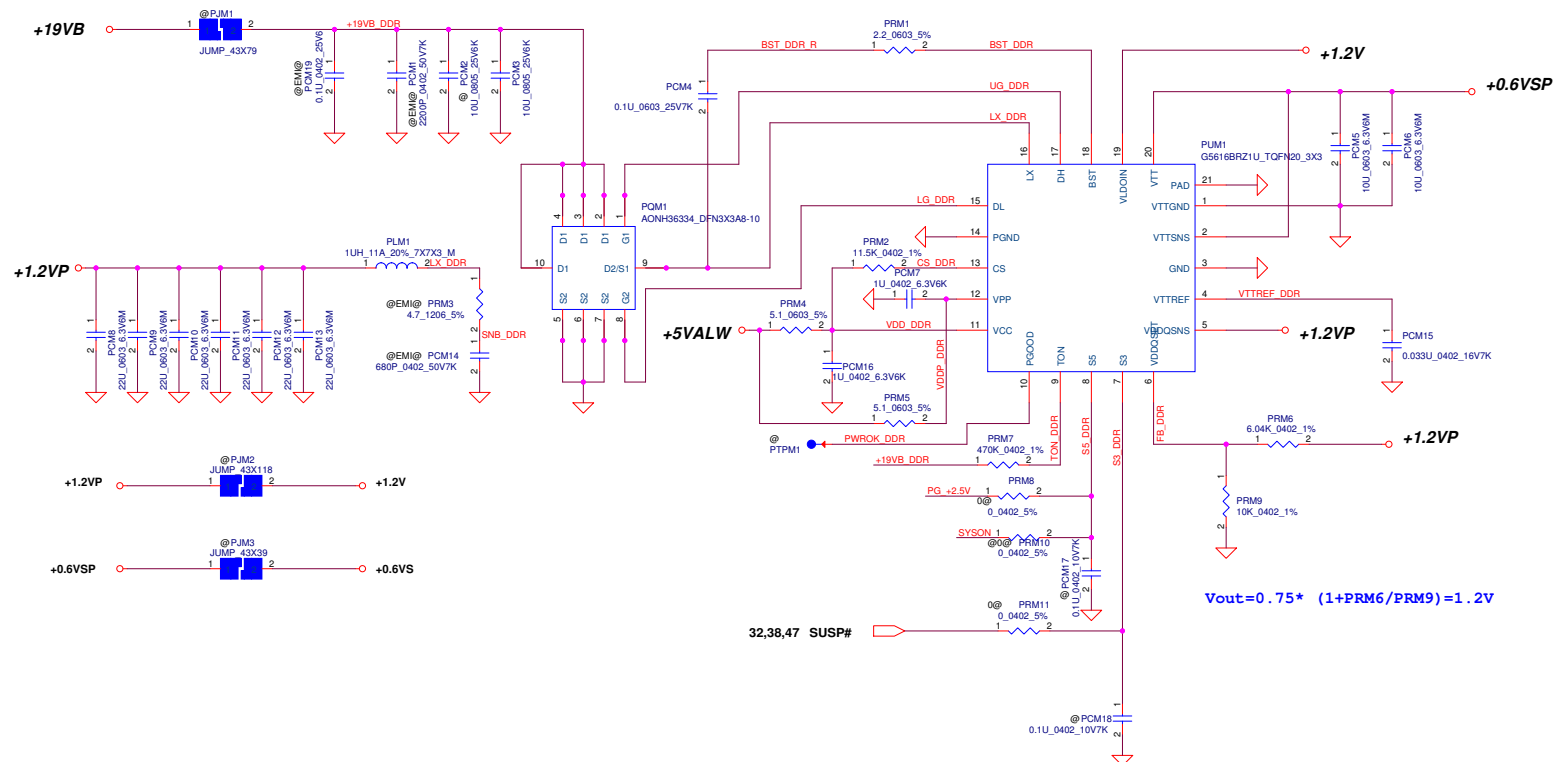
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2015/09/01	Deciphered Date	2018/09/01	Title	BATT Conn
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Intel / Gemini Lake
Date:	Thursday, November 23, 2017	Sheet	41	of	53

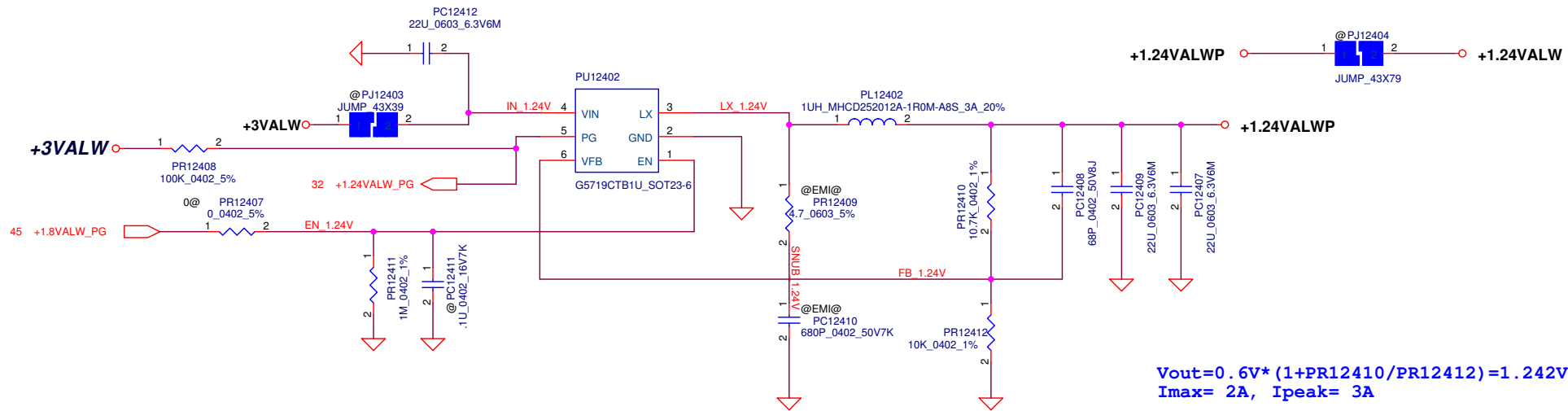


THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Document Number		Rev
Intel / Gemini Lake		0.1
Date:	Thursday, November 23, 2017	Sheet 42 of 53





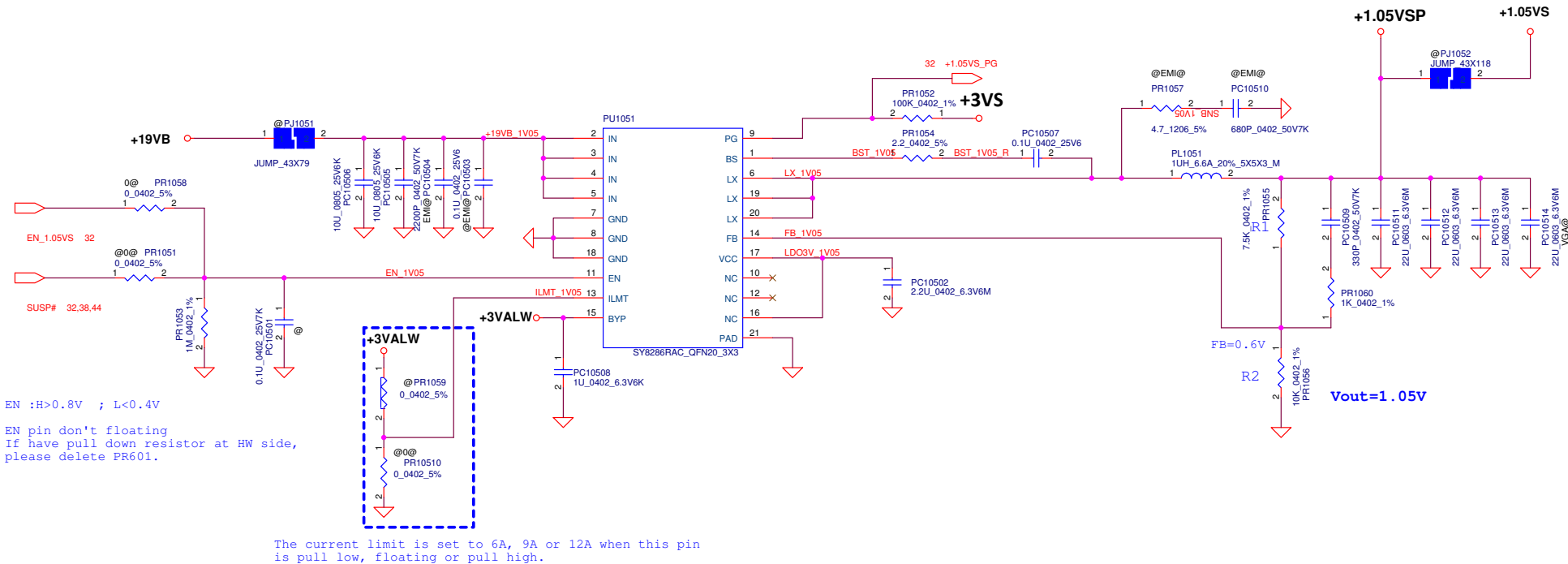


Security Classification		Compal Secret Data		Title	
Issued Date	2015/09/01	Deciphered Date	2018/09/01	1.24VALWP	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				Custom	0.1
				Date:	Thursday, November 23, 2017
				Sheet	46 of 53

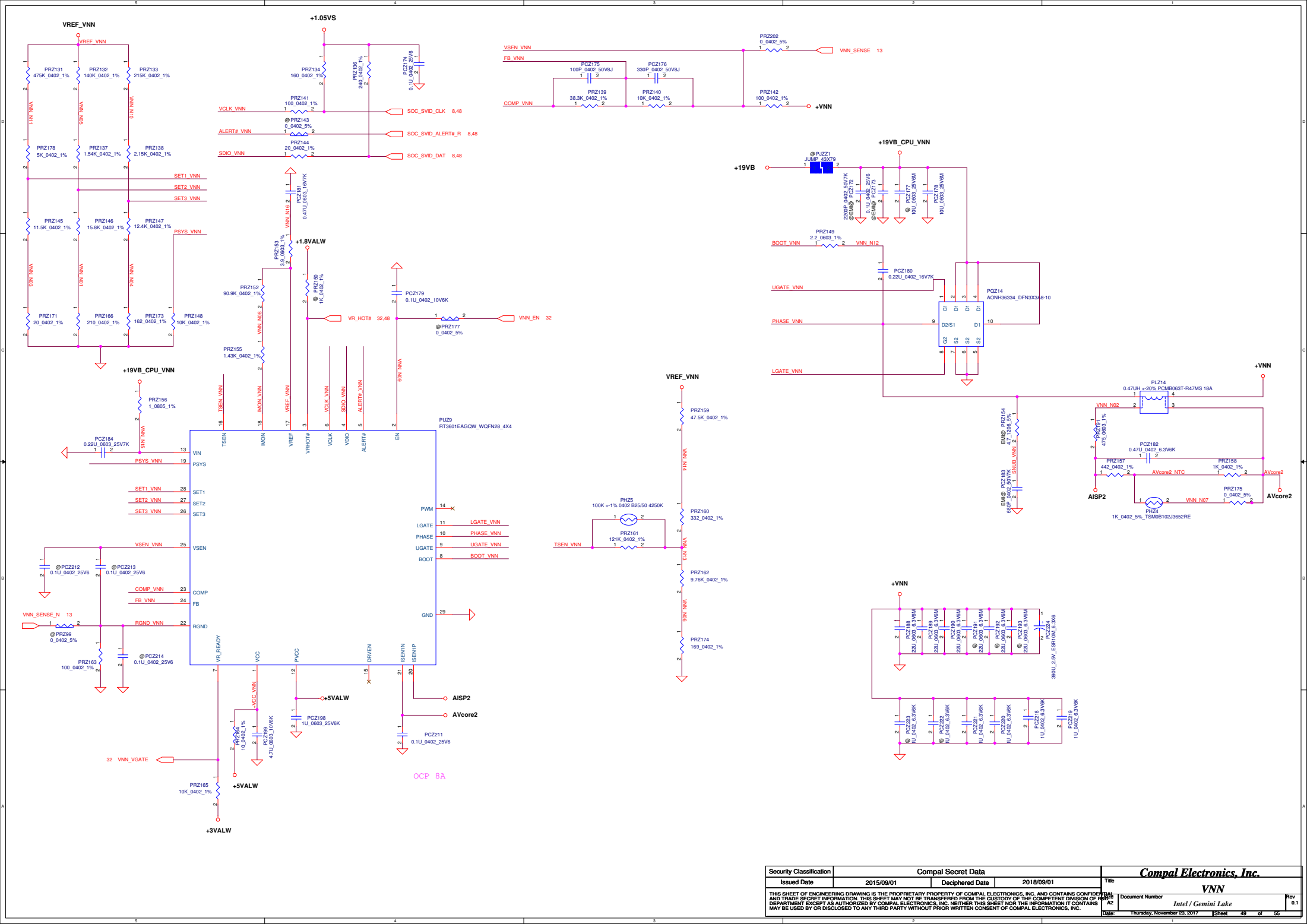
Compal Electronics, Inc.

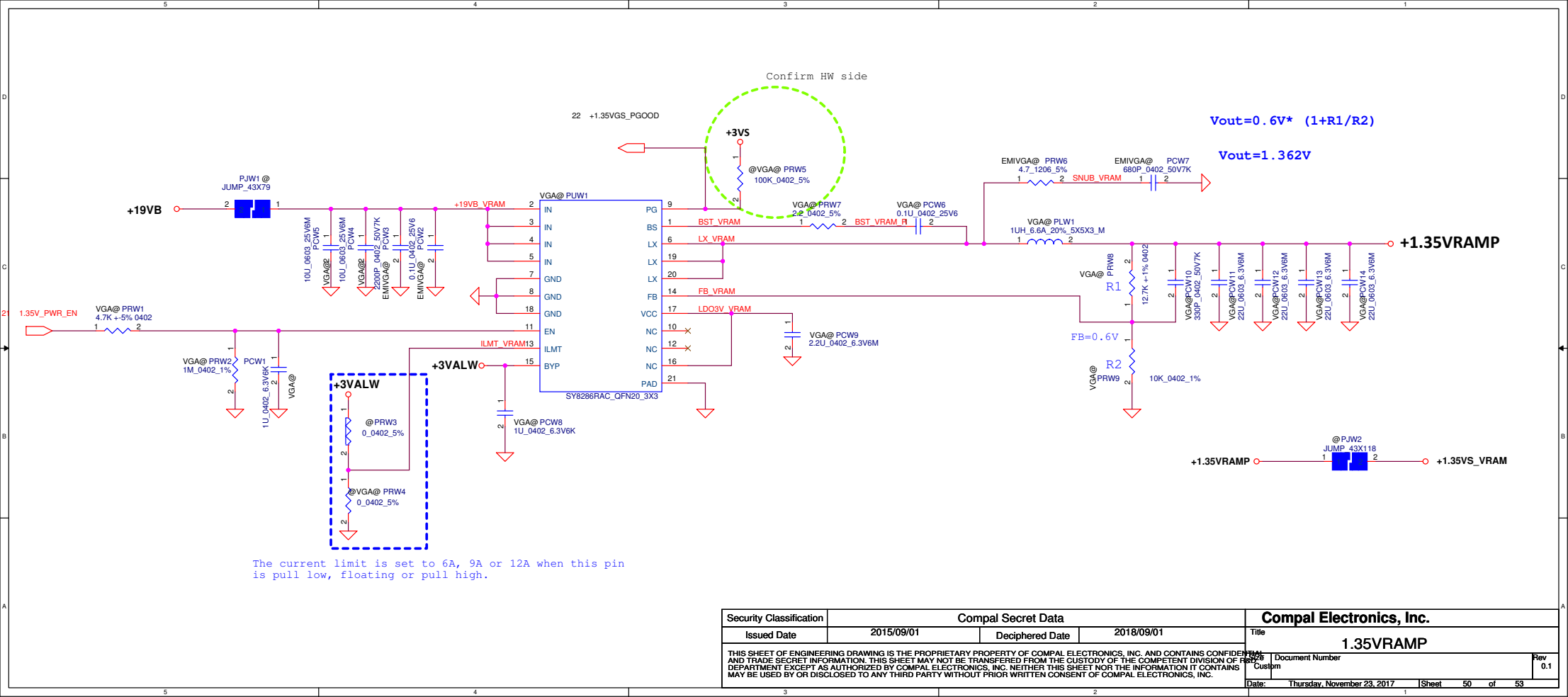
1.24VALWP

Intel / Gemini Lake



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/09/01	Deciphered Date	2018/09/01	Title	1.05V
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 0.1
				Date:	Thursday, November 23, 2017
				Sheet	47 of 53

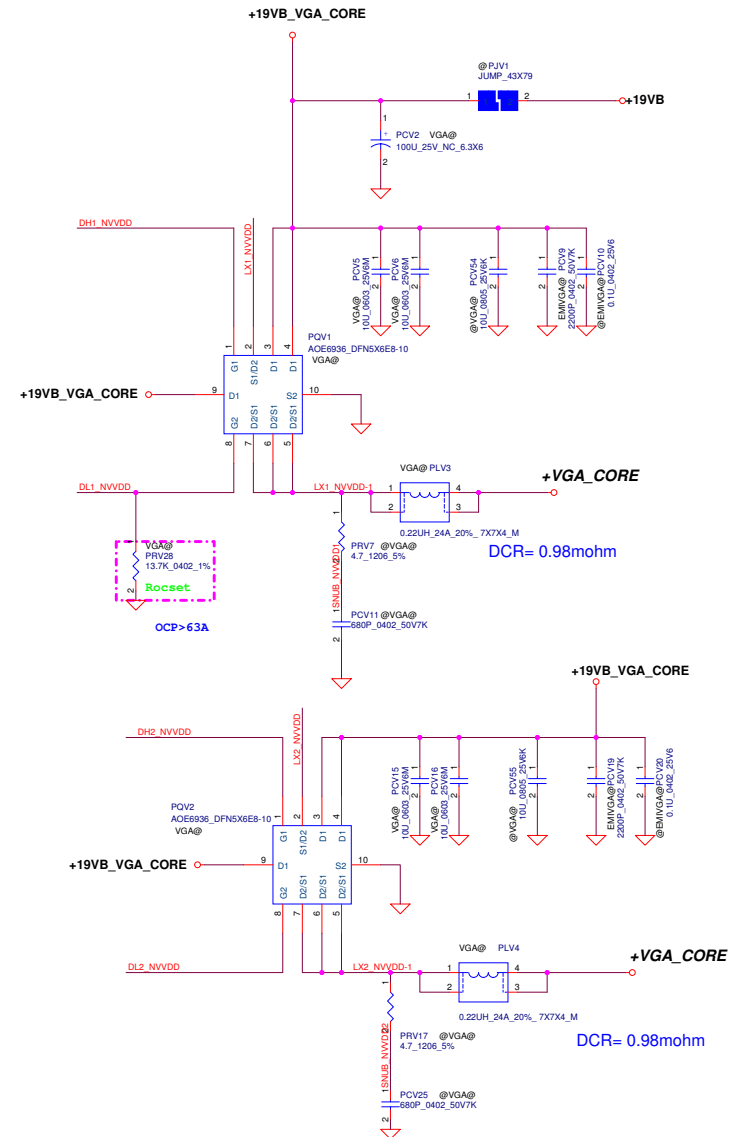
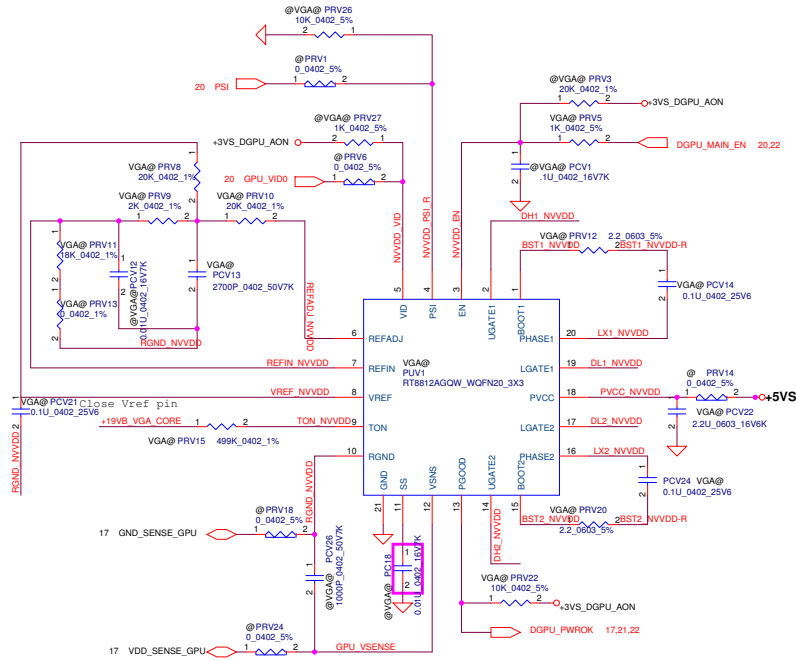




Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/09/01	Deciphered Date	2018/09/01	Title	1.35VRAMP
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 0.1
Date: Thursday, November 23, 2017				Sheet	50 of 53

PWM-VID Spec		Config B
Vmin		0.6V
Vmax		1.2V
Vboot		0.9V
Voltage		6.25mV
N59 Voltage level		96
Rrefadj	PRV10	20K
Rref1	PRV8	20K
Rboot	PRV9	2K
Rref2=PRV8+PRV11	PRV11	18K
	PRV13	0
C	PCV13	2.7nf

VGA Chip	N16S-GTR
OpenVReg Configurations	Config B
Rated TDP Power at 25°C	18W
Power GPU Total at Tj=102C	23W
EDP-Continuous at Tj=102C	26A
EDP-Peak at Tj=102C	51A
Istep max (Evaluation)	36.36A
OCF Setting	61A
Reboot	9.76K
Recommendation	Zphase



Security Classification	Compal Secret Data		Title	
Issued Date	2015/09/01	Deciphered Date	2018/09/01	VGA CORE Document Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. THIS SHEET MAY NOT BE REPRODUCED OR THE CUSTODY OF THE COMPETENT DIVISION OR GROUP DEPARTMENTS EXCEPT AS REQUIRED BY COMPAL ELECTRONICS, INC. WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev 0.1
Date:	Thursday, November 23, 2017	Sheet	51	of 53

[illegible]